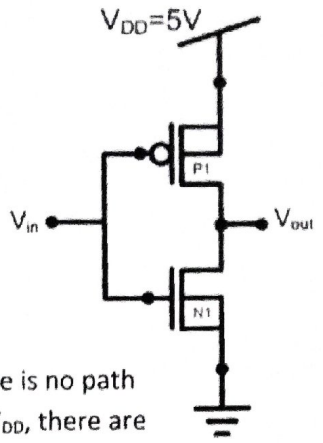
Practice 5: CMOS Inverter

Exercise 1



The following CMOS inverter has these parameters:

$$V_{Tn}=1V \quad V_{Tp}=-1.5V \quad k_n=100\frac{\mu A}{V^2} \quad k_p=50\frac{\mu A}{V^2}$$

Find Nominal Voltage Levels and draw the VTC.

Solution:

1. We'll start with V_{in}=0. In this case, N1 is cut-off and there is no path to ground, so after filling up an output capacitance to V_{DD}, there are no static currents. $V_{OHmax}=V_{DD}$.
2. As we raise V_{in}, N1 stays in cut-off until $V_{in}=V_{GS}>V_T$. On the other hand, P1 is open ($V_{SG}\rightarrow V_{DD}$) with a low voltage across its output ($V_{SD}\rightarrow 0$), meaning we are in the linear region.

   $$I_{Dp}=k_p\left[\left(V_{SGp}-\left|V_{Tp}\right|\right)V_{SDp}-{V_{SDp}}^2\right]$$
3. Once $V_{in}>V_{Tn}$, N1 starts conducting in the saturation region. To find V_{OHmin} and V_{IL}, we will first equate the two currents and then look for the point where gain=-1 by differentiating:

   $$I_{Dp}=k_p\left[\left(V_{SGp}-\left|V_{Tp}\right|\right)V_{SDp}-\frac{{V_{SDp}}^2}{2}\right]=k_p\left[\left(V_{DD}-V_{in}-\left|V_{Tp}\right|\right)\left(V_{DD}-V_{out}\right)-\frac{\left(V_{DD}-V_{out}\right)^2}{2}\right]$$

   $$I_{Dn}=\frac{k_n}{2}\left(V_{GSn}-V_{Tn}\right)^2\left(1+\lambda V_{DS}\right)\approx\frac{k_n}{2}\left(V_{in}-V_{Tn}\right)^2$$

   $$I_{Dp}=I_{Dn}=50\left[\left(3.5-V_{in}\right)\left(5-V_{out}\right)-\frac{\left(5-V_{out}\right)^2}{2}\right]=50\left(V_{in}-1\right)^2$$

   $$5-5V_{in}+1.5V_{out}+V_{in}V_{out}-0.5{V_{out}}^2={V_{in}}^2-2V_{in}+1$$

   We'll differentiate both sides by dV_{in}:

   $$-5+1.5\frac{dV_{out}}{dV_{in}}+V_{out}+V_{in}\frac{dV_{out}}{dV_{in}}-V_{out}\frac{dV_{out}}{dV_{in}}=2V_{in}-2$$

   Now we'll substitute $\frac{dV_{out}}{dV_{in}}=-1$ and get: $V_{in}=\frac{2V_{out}-4.5}{3}$

   We'll put V_{in} back in the original equation and get:

   $$5-5\frac{2V_{out}-4.5}{3}+1.5V_{out}+\frac{2V_{out}-4.5}{3}V_{out}-0.5{V_{out}}^2=\left(\frac{2V_{out}-4.5}{3}-1\right)^2$$

   $$12.5-\frac{10}{3}V_{out}+\frac{1}{6}{V_{out}}^2=\frac{4}{9}{V_{out}}^2-\frac{10}{3}V_{out}+6.25$$

   $${V_{out}}^2=22.5 \quad V_{OH\,min}=4.7V \quad V_{IL}=1.66V$$

In the same fashion, we'll find V_{OLmax} and V_{IH}, though this time, P1 is saturated and N1 is linear:

$$I_{Dn} = k_n\left[(V_{GSn} - V_{Tn})V_{DSn} - \frac{V_{DSn}^2}{2}\right] = k_n\left[(V_{in} - V_{Tn})V_{out} - \frac{V_{out}^2}{2}\right]$$

$$I_{Dp} = \frac{k_p}{2}\left(V_{SGp} - |V_{Tp}|\right)^2\left(1 + \lambda V_{SDp}\right) \approx \frac{k_p}{2}\left(V_{DD} - V_{in} - |V_{Tp}|\right)^2$$

$$I_{Dn} = I_{Dp} = 100\left[(V_{in} - 1)V_{out} - \frac{V_{out}^2}{2}\right] = 25(5 - V_{in} - 1.5)^2$$

$$4\left(V_{in}V_{out} - V_{out} - 0.5V_{out}^2\right) = 12.25 - 7V_{in} + V_{in}^2$$

Differentiating and substituting $\frac{dV_{out}}{dV_{in}} = -1$ gives us:

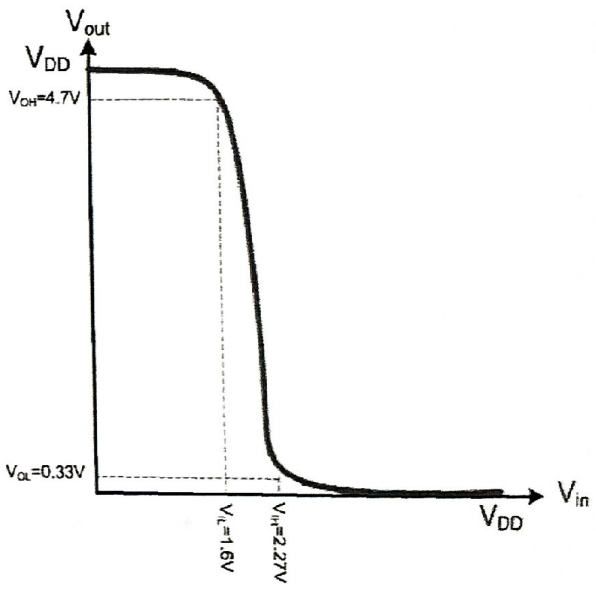
$$4\left(V_{out} + V_{in}\frac{dV_{out}}{dV_{in}} - \frac{dV_{out}}{dV_{in}} - V_{out}\frac{dV_{out}}{dV_{in}}\right) = 2V_{in} - 7 \qquad V_{in} = \frac{8V_{out} + 11}{6}$$

Substituting into the original equation:

$$4\left(\frac{8V_{out} + 11}{6}V_{out} - V_{out} - 0.5V_{out}^2\right) = \left(3.5 - \frac{8V_{out} + 11}{6}\right)^2$$

$$\frac{14}{9}V_{out}^2 + \frac{70}{9}V_{out} - \frac{25}{9} = 0 \qquad V_{OL\max} = 0.33 \qquad V_{IH} = 2.27$$

4. Finally, when V_{in}=5V, P1 is cut-off and there is no path to V_{DD}, so after discharging the output capacitance, there are no static currents. V_{OLmin}=0V
5. We can now draw the VTC:



Exercise 2: Propagation Delay

Given an inverter with the following properties:

$$\frac{(W/L)_p}{(W/L)_n} = 3.4 \quad L_{\min} = 0.25\mu m \quad (W/L)_{\min} = 1.5 \text{ } \textit{(Assume long channel)}$$

fabricated in an 0.25µm process with the following process characteristics:

V_{DD}=2.5V	$V_{T0}[V]$	$\gamma[\sqrt{V}]$	$k'\left[\mu A/V^2\right]$	$\lambda[V^{-1}]$
nMOS	0.43	0.4	115	0.06
pMOS	-0.4	-0.4	-30	-0.1

Derive the High to Low propagation delay (t_{pHL}) driving a 50fF capacitance.