University of M'sila

Faculty of Technology

Electronic Department

1st year Master Microelectronics

Course: Design of MOS analog integrated circuits

Chapter I: Introduction to MOS Transistor

1. Introduction

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a key component in modern electronics and is widely used in integrated circuits. It is a type of transistor that uses an electric field to control the flow of current. MOSFETs are known for their high input impedance, low power consumption, and fast switching speeds.

Metal Oxide Semiconductor is a three terminal device having source, drain and gate (Figure 1). The resistance path between the drain and the source is controlled by applying a voltage to the gate. The Normal conduction characteristics of a MOS transistor can be categorized as cut-off region Non saturated region and saturated region.

MOSFETs are further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation; the name MOSFET stands for metal–oxide–semiconductor field-effect transistor. Since there are differences in the characteristics and operation of different types of MOSFET, they are covered in separate sections.

2. Different Transistor Types

MOSFET transistors are divided in two types: PMOS and NMOS, depending on the substrate used**.** The primary distinction between PMOS and NMOS is in the two systems' various structures. While NMOS uses N-type doped semiconductors as source and drain and P-type as the substrate, those of a PMOS device are the reverse. When exposed to a non-negligible voltage, an NMOS (negative-MOS) transistor creates a closed circuit; when exposed to a voltage of about 0 volts, it makes an open circuit. A PMOS (positive-MOS) transistor forms an open circuit when it gets a non-negligible voltage and a closed circuit when it receives a voltage of about 0 volts. NMOS is more frequently employed than PMOS because of its advantages, however, PMOS is still needed in many applications because of its polarization characteristics.

3. Enhancement-type MOSFET: Device structure and operation

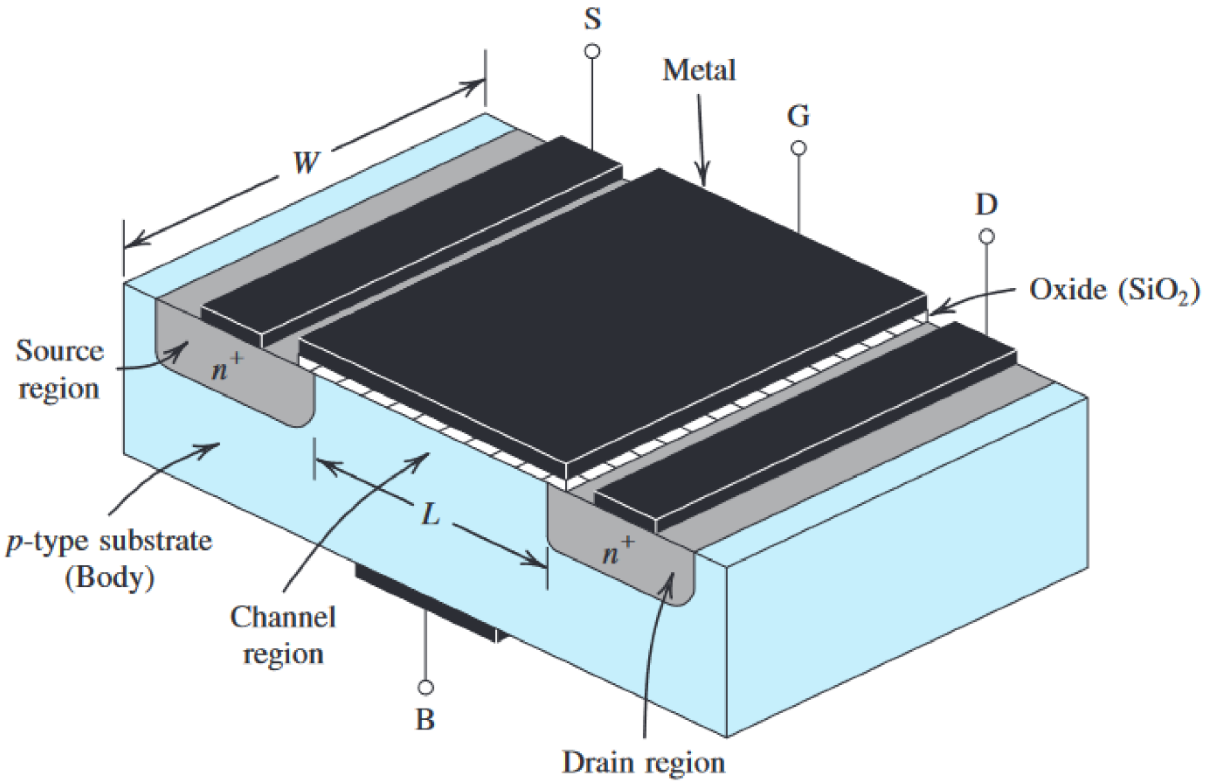
This section is devoted to the study of the enhancement-type MOSFET only. We begin by learning about its structure and physical operation. This will lead to the current–voltage characteristics of the device.

Figure 1 shows the physical structure of the n-channel enhancement-type MOSFET (PMOS). The transistor is fabricated on a p-type substrate, which is a single-crystal silicon wafer that provides physical support for the device, Two heavily doped n-type regions, indicated in the figure as the n+ source and the n+ drain regions, are created in the substrate. A thin layer of silicon dioxide (SiO2) of thickness tox (typically 1 nm to 10 nm), which is an excellent electrical insulator, is grown on the surface of the substrate, covering the area between the source and drain regions. Metal is deposited on top of the oxide layer to form the gate electrode of the device. Metal contacts are also made to the source region, the drain region, and the substrate, also known as the body.

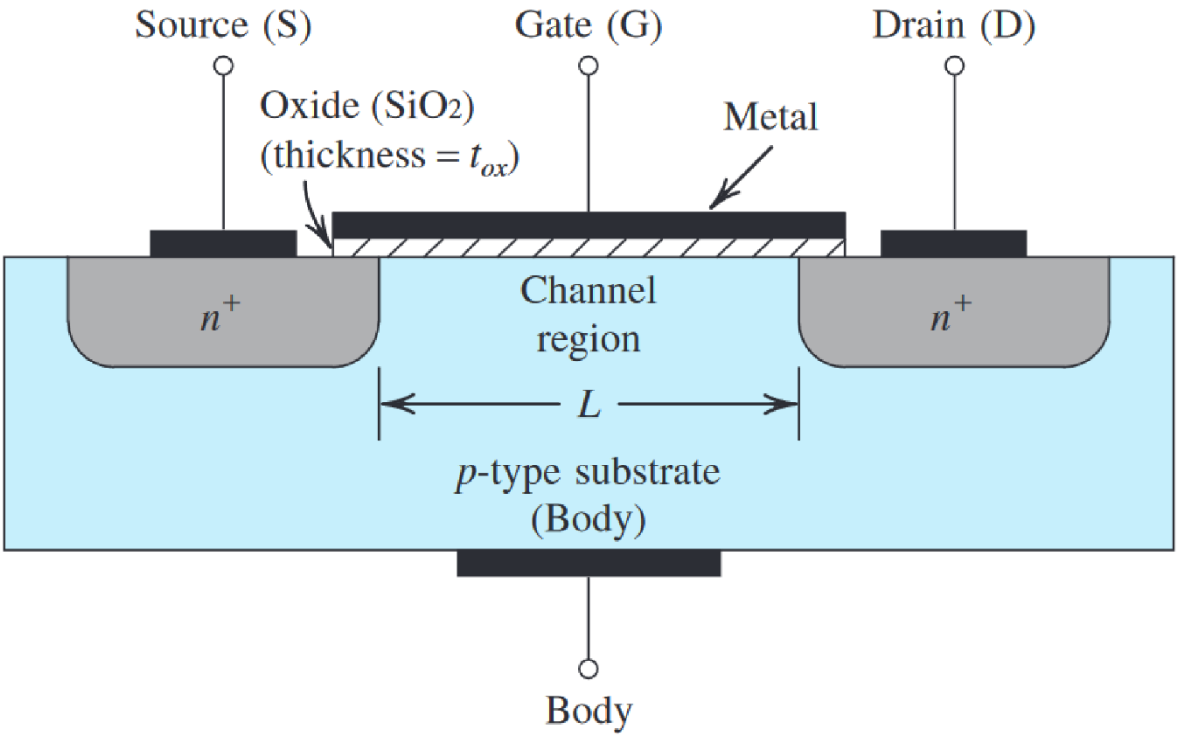
Thus four terminals are brought out:

- the gate terminal (G),
- the source terminal (S),
- the drain terminal (D),
- and the substrate or body terminal (B).

At this point it should be clear that the name of the device (**metal-oxide-semiconductor FET**) is derived from its physical structure.



(a)



(B)

(b)

Figure 1: Physical structure of the enhancement-type NMOS transistor: (a) perspective view (3D); (b) cross-section (2D). (Typically, L = 0.03 μm to 1 μm, W = 0.05 μm to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10 nm.)

3.1 Operation with Zero Gate Voltage

With zero voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the pn junction between the n+ drain region and the p-type substrate, and the other diode is formed by the pn junction between the p-type substrate and the n+ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage V_{DS} is applied. In fact, the path between drain and source has a very high resistance (of the order of 10^{12} Ω).

3.2 Creating a Channel for Current Flow

Consider next the situation depicted in Figure I.2. Here we have grounded the source and the drain and applied a positive voltage to the gate. Since the source is grounded, the gate voltage appears in effect between gate and source and thus is denoted v_{GS}.

The positive voltage on the gate causes, in the first instance, the free holes (which are positively charged) to be repelled from the region of the substrate under the gate (the channel region). These holes are pushed downward into the substrate, leaving behind a **carrier-depletion region**. The depletion region is populated by the bound negative charge associated with the acceptor atoms.

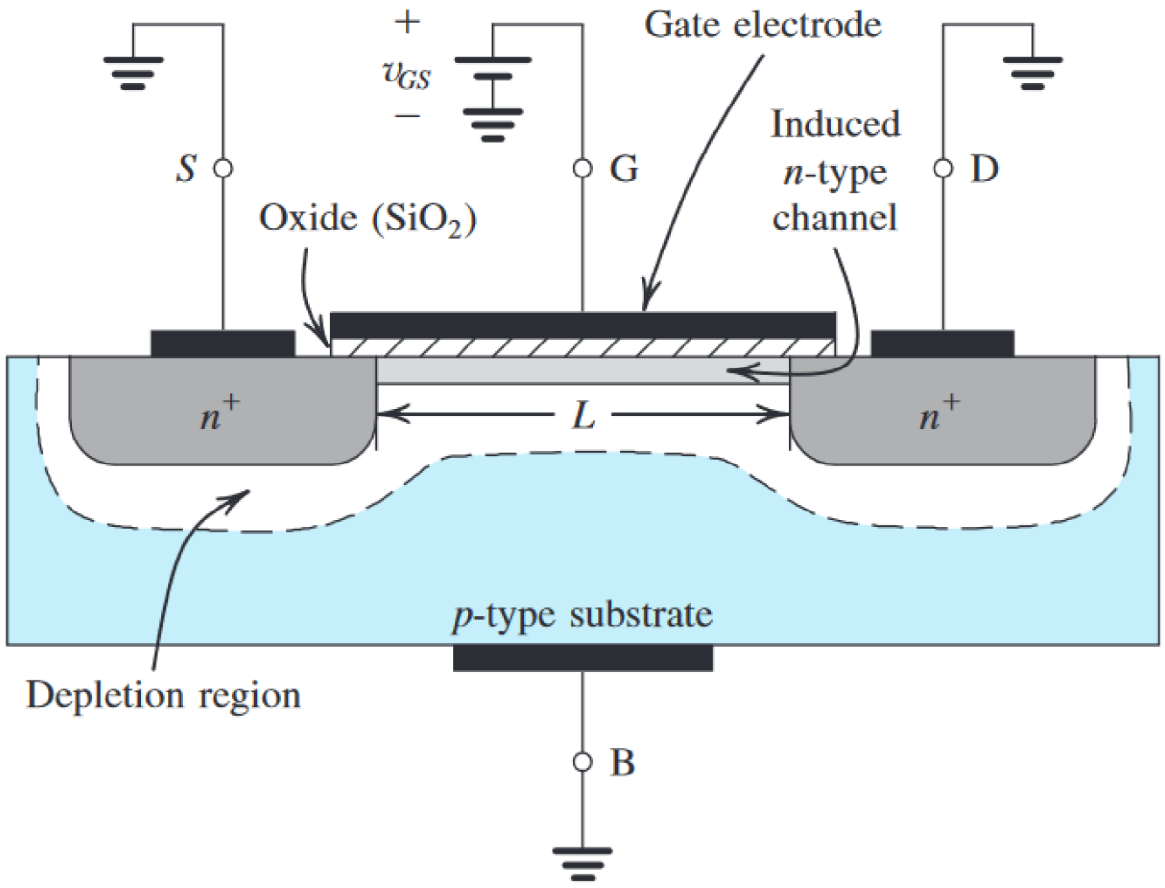


Figure 2: The enhancement-type NMOS transistor with a positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate.

When a sufficient number of electrons accumulate near the surface of the substrate under the gate, an n region is in effect created, connecting the source and drain regions, as indicated in Figure 2.

If a voltage is applied between drain and source, current flows through this induced n region, carried by the mobile electrons. The induced n region thus forms a **channel** for current flow from drain to source and is aptly called an **n-channel MOSFET** or, alternatively, **an NMOS transistor**, as indicated in Figure I.2. Note that:

- An n-channel MOSFET is formed in a p-type substrate.
- The channel is created by inverting the substrate surface from p type to n type.
- Hence the induced channel is also called **an inversion layer**.
- The value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called **the threshold voltage** and is denoted Vth.
- The value of V_{th} is controlled during device fabrication and typically lies in the range of 0.3 Volt to 1.0 Volt.
- The gate and the channel region of the MOSFET form a parallel-plate capacitor.

- The positive gate voltage causes positive charge to accumulate on the top plate of the capacitor (the gate electrode).
- The corresponding negative charge on the bottom plate is formed by the electrons in the induced channel.
- An electric field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel, and thus it determines the channel conductivity and, in turn, the current that will flow through the channel when a voltage VDS is applied. This is the origin of the name "field-effect transistor" (FET).
- The voltage across this parallel-plate capacitor must exceed Vth

The excess of V_{GS} over V_{th} is termed **the effective voltage** or **the overdrive voltage (V_{ov})**:

$$V_{ov} = V_{GS} - V_{th} \quad (1)$$

We can express the magnitude of the electron charge in the channel by:

$$|Q| = C_{ox}(WL)v_{ov} \quad (2)$$

where C_{ox}, called **the oxide capacitance**, is the capacitance of the parallel-plate capacitor per unit gate area (in units of F/m^2), W is the **width of the channel**, and L is the **length of the channel**. The oxide capacitance C_{ox} is given by:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (3)$$

where ε_{ox} is the **permittivity** of the silicon dioxide, so:

$$\varepsilon_{ox} = 3.9\ \varepsilon_o = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11}\ \text{F/m}$$

The **oxide thickness** t_{ox} is determined by the process technology used to fabricate the MOSFET. As an example, for a process with t_{ox} = 4 nm:

$$C_{ox} = \frac{3.45 \times 10^{-11}}{4 \times 10^{-9}} = 8.6 \times 10^{-3}\ F/m$$

For a MOSFET fabricated in this technology with a channel length L = 0.18 μm and a channel width W = 0.72 μm, the total capacitance between gate and channel is:

$$C = C_{ox}\ WL = 8.6 \times 0.18 \times 0.72 = 1.1\ \text{fF}$$

3.3 Applying a Small V_{DS}

We now apply a positive voltage V_{DS} between drain and source, as shown in Figure I.3. We first consider the case where V_{DS} is small (i.e., 50 mV or so), to have induced a channel.

The voltage V_{DS} causes a current I_D to flow through the induced **n channel**. Current is carried by free electrons traveling from source to drain. By convention, the direction of current flow is opposite to that of the flow of negative charge. Thus the current in the channel, I_D, will be from drain to source, as indicated in Figure I.3.

To calculate the value of I_D, we assume that the voltage V_{DS} is small, and the voltage between the gate and various points along the channel remains approximately constant and equal to the value at the source end, V_{GS} and the effective voltage between the gate and the various points along the channel remains equal to V_{OV}.

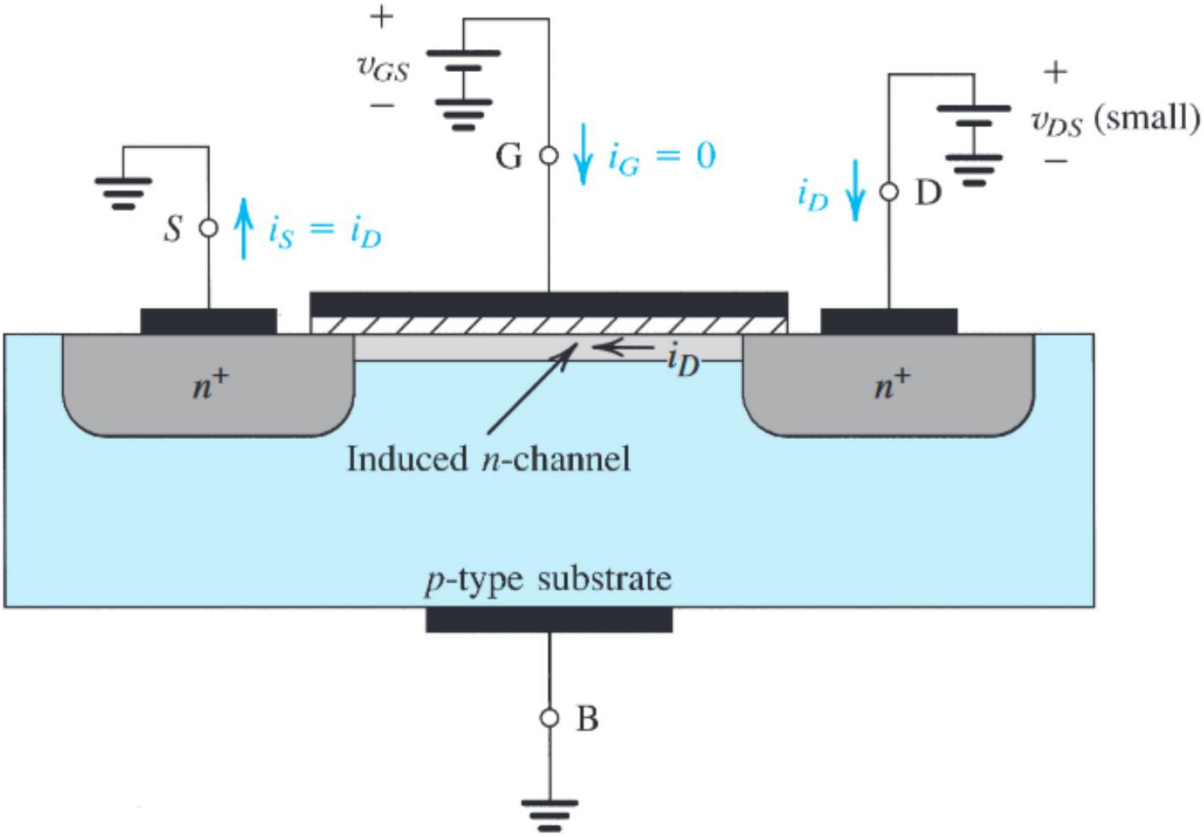


Figure 3: An NMOS transistor with $V_{GS} > V_{th}$ and with a small V_{DS} applied. The device acts as a resistance whose value is determined by V_{GS}. Specifically, the channel conductance is proportional to $V_{GS} – V_{th}$, and thus I_d is proportional to $(V_{GS} – V_{th})V_{DS}$. Note that the depletion region is not shown (for simplicity).

The **channel charge** Q is still given by Equation (2). Of particular interest in calculating the current I_D is the charge per unit channel length, which can be found from Equation (2) as:

$$\frac{|Q|}{Unit\ channel\ length} = C_{ox}WV_{ov} \tag{4}$$

The voltage V_{DS} establishes an **electric field** E across the length of the channel:

$$|E| = \frac{V_{DS}}{L} \tag{5}$$

This electric field in turn causes the channel electrons to drift toward the drain with a **velocity** given by:

$$Electron\ drift\ velocity = \mu_n \frac{V_{DS}}{L} \tag{6}$$

where μ_n is the **mobility of the electrons** at the surface of the channel. It is a physical parameter whose value depends on the fabrication process technology. The value of I_D can now be found by multiplying the charge per unit channel length (Equation 4) by the electron drift velocity (Equation 6), so:

$$I_D = \left[\mu_n C_{ox}\left(\frac{W}{L}\right)V_{ov}\right]V_{DS} \tag{7}$$

For small V_{DS} , the channel behaves as a linear resistance whose value is controlled by the overdrive voltage V_{ov} , which in turn is determined by V_{GS} :

$$I_D = \left[\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th})\right]V_{DS} \tag{8}$$

The **conductance** g_{DS} of the channel can be found from Equation (7) or (8) as:

$$g_{DS} = \mu_n C_{ox}\left(\frac{W}{L}\right)V_{ov} \tag{9}$$

Or

$$g_{DS} = \mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th}) \tag{10}$$

a) The first Factor ($\mu_n C_{ox}$) is termed **the process transconductance parameter** and given the symbol k'_n, where the subscript n denotes n channel:

$$K'_n = \mu_n C_{ox} \tag{11}$$

b) The second factor in the expression for the conductance g_{DS} in equation (9) and (10) is the **transistor aspect ratio** (W/L). The product of the process transconductance parameter k'_n and the transistor aspect ratio (W/L) is **the MOSFET transconductance parameter** k_n :

$$K_n = K'_n(W/L) \tag{12a}$$

Or

$$K_n = \mu_n C_{ox}(W/L) \tag{12b}$$

The MOSFET parameter k_n has the dimensions of A/V^2.

c) The third term in the expression of the channel conductance g_{DS} is the overdrive voltage V_{OV}. The V_{OV} directly determines the magnitude of electron charge in the channel. As will be seen, V_{OV} is a very important circuit-design parameter. In this section we will use V_{OV} and $V_{GS} - V_{th}$ interchangeably. With V_{DS} kept small, the MOSFET behaves as a linear resistance r_{DS} whose value is controlled by the gate voltage V_{GS} :

$$r_{DS} = \frac{1}{g_{DS}} \tag{13}$$

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)v_{ov}} \tag{13a}$$

$$r_{DS} = \frac{1}{(\mu_n C_{ox})(W/L)(v_{GS} - v_{th})} \tag{13b}$$

With increasing V_{GS} above the threshold voltage V_{th} enhances the channel, hence the names **enhancement-mode operation** and **enhancement-type MOSFET**. Finally, we note that the current that leaves the source terminal (I_S) is equal to the current that enters the drain terminal (I_D), and the gate current $I_G = 0$.

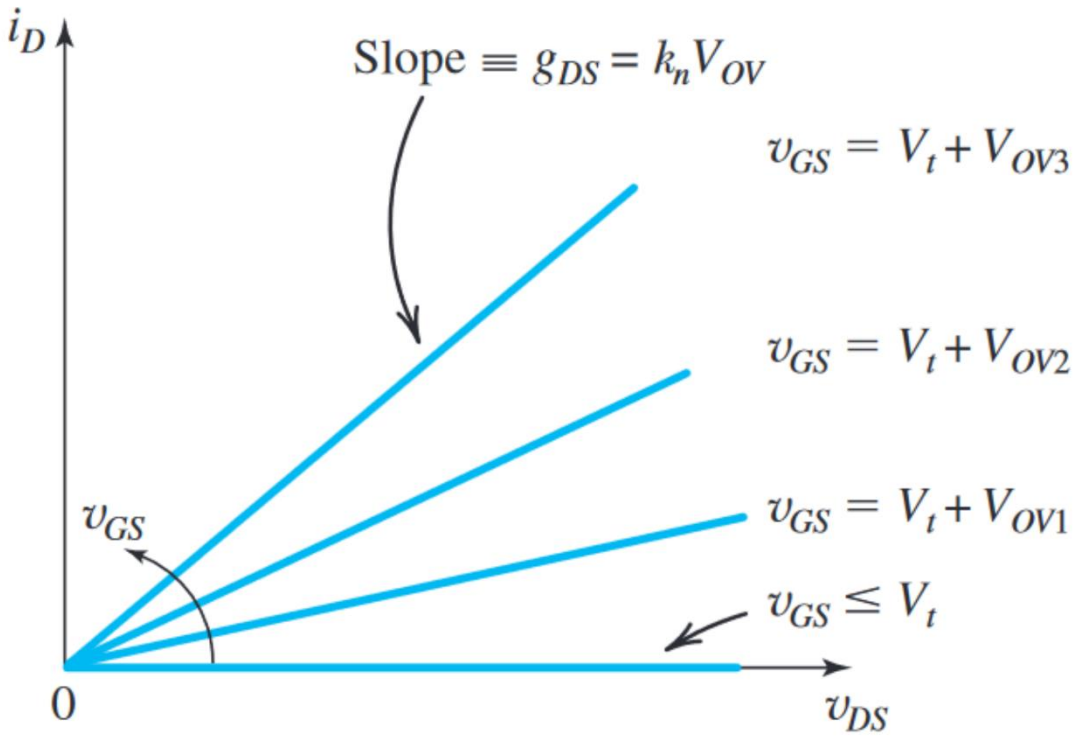


Figure 4: The $I_D - V_{DS}$ characteristics of the MOSFET in Figure 3 when the voltage applied between drain and source, V_{DS}, is kept small. The device operates as a linear resistance whose value is controlled by V_{GS}.

Exercice 1: A 0.18-μm fabrication process is specified to have t_{ox} = 4 nm, μ_n = 450 cm^2/V·s, and V_{th} = 0.5 V.

a-Find the value of the process transconductance parameter k'_n. For a MOSFET with minimum length fabricated in this process,

b-Find the required value of W so that the device exhibits a channel resistance r_{DS} of 1 kΩ at V_{GS} = 1 V.

Answer (a) 388 μA/V^2 ; (b) 0.93 μm.

3.4 Operation as V_{DS} is Increased

- Let V_{GS} be held constant at a value greater than V_{th},
- Let the MOSFET be operated at a constant overdrive voltage V_{OV}.
- Note that V_{DS} appears as a voltage drop across the length of the channel.

- The voltage (measured relative to the source) increases from zero to V_{DS}. Thus the voltage between the gate and points along the channel decreases from $V_{GS} = V_{th} + V_{OV}$ at the source end to $V_{GD} = V_{GS} - V_{DS} = V_{th} + V_{OV} - V_{DS}$ at the drain end.

we find that the channel will take the **tapered shape** shown in Figure 5, being deepest at the source end (where the depth is proportional to V_{OV}) and shallowest at the drain end (where the depth is proportional to $V_{OV} - V_{DS}$). This point is further illustrated in Figure 6.

As V_{DS} is increased, the channel becomes **more tapered** and its resistance increases correspondingly. Thus, the $I_D - V_{DS}$ curve does not continue as a straight line but bends as shown in Figure 7. The equation describing this portion of the $I_D - V_{DS}$ curve can be easily derived by utilizing the information in Figure 6. Specifically, note that the charge in the tapered channel is proportional to the channel cross-sectional area shown in Figure 6(b). This area in turn can be easily seen as proportional to $\frac{1}{2}[V_{OV} + (V_{OV} - v_{DS})]$or $\left(V_{OV} - \frac{1}{2}v_{DS}\right)$. Thus, the relationship between I_D and V_{DS} can be found by replacing V_{OV} in Equation (7) by $\left(V_{OV} - \frac{1}{2}v_{DS}\right)$ thus:

$$i_D = K_n' \left(\frac{W}{L}\right)\left(V_{OV} - \frac{1}{2}v_{DS}\right)v_{DS} \qquad (14)$$

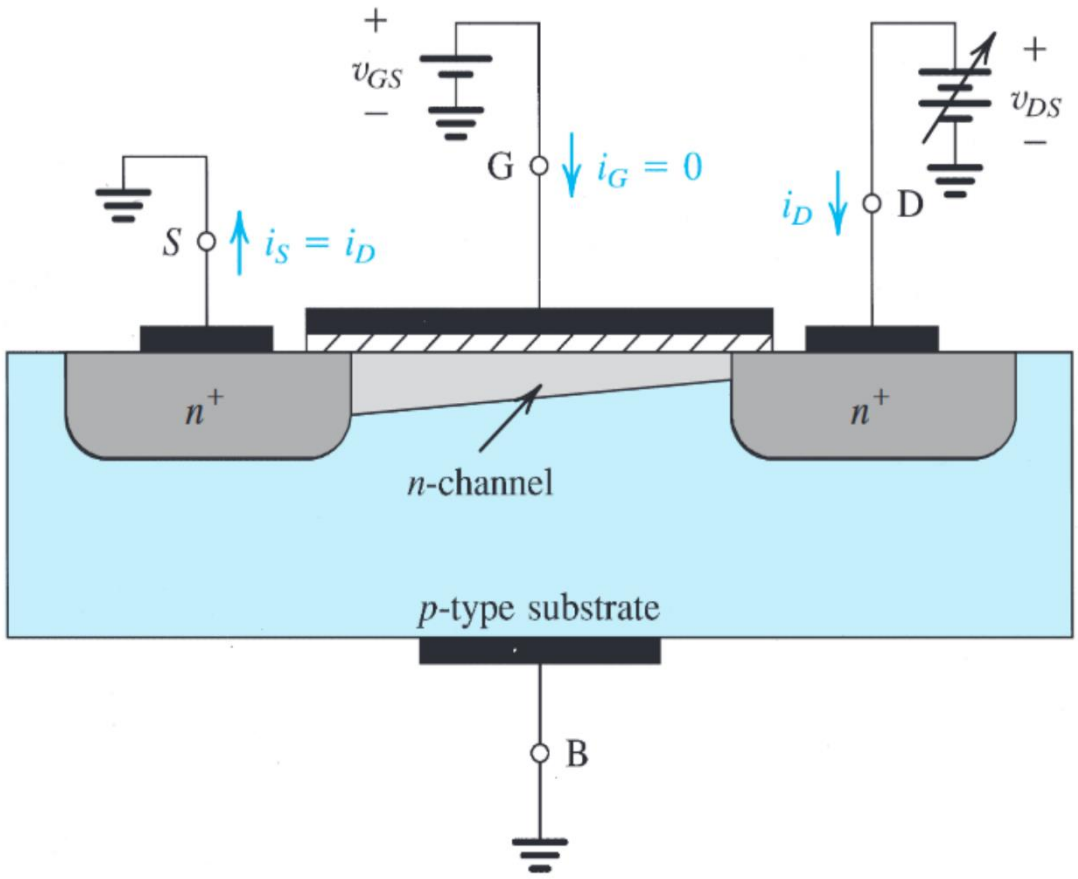


Figure 5: Operation of the enhancement NMOS transistor as V_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as V_{DS} is increased. Here, V_{GS} is kept constant at a value > V_{th} ; $V_{GS} = V_{th} + V_{OV}$.

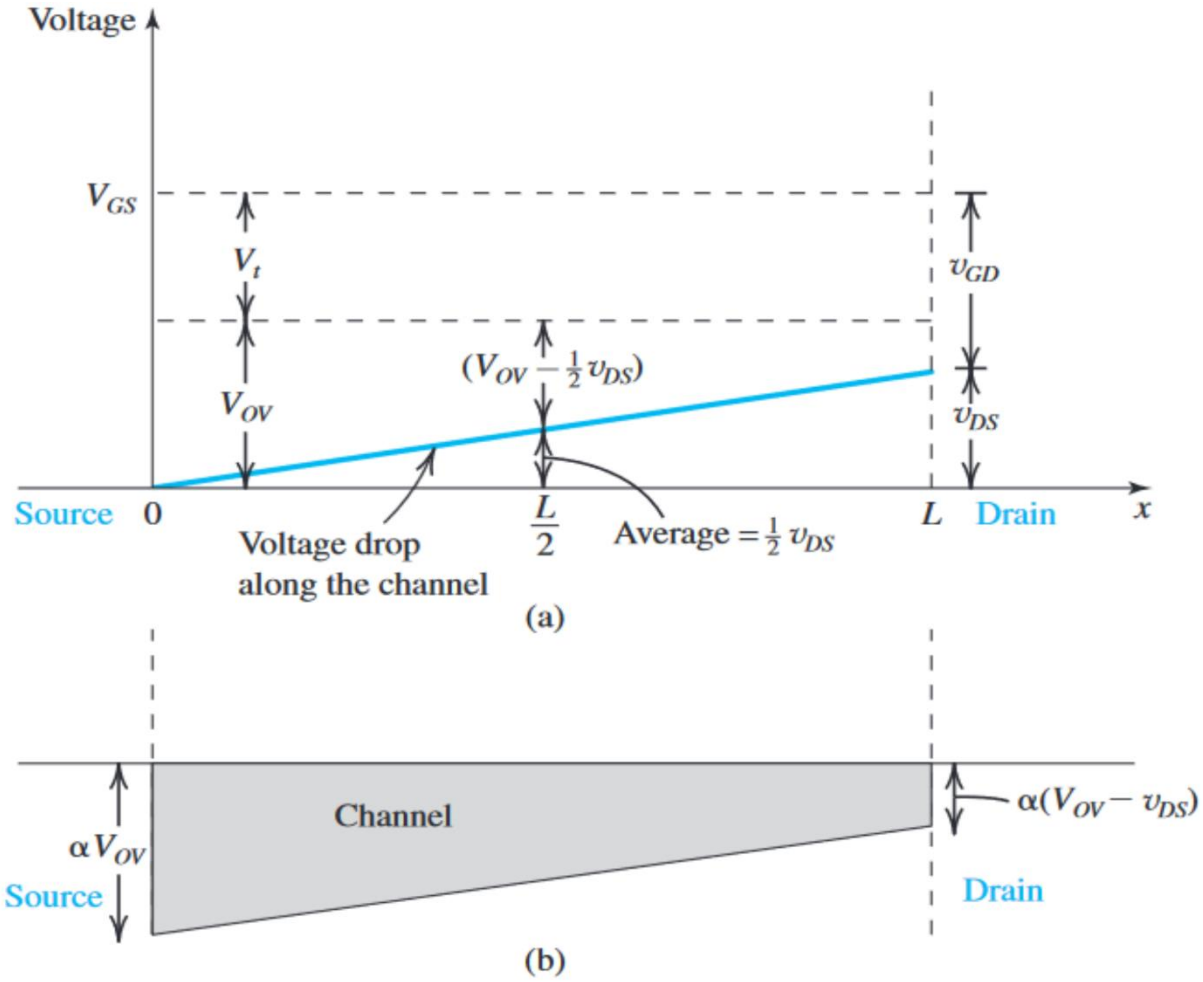


Figure 6: (a) For a MOSFET with $V_{GS} = V_{th} + V_{OV}$, application of V_{DS} causes the voltage drop along the channel to vary linearly, with an average value of $1/2V_{DS}$ at the midpoint. Since $V_{GD}>V_{th}$, the channel still exists at the drain end. (b) The channel shape corresponding to the situation in (a). While the depth of the channel at the source end is still proportional to V_{OV}, that at the drain end is proportional to $(V_{OV} - V_{DS})$.

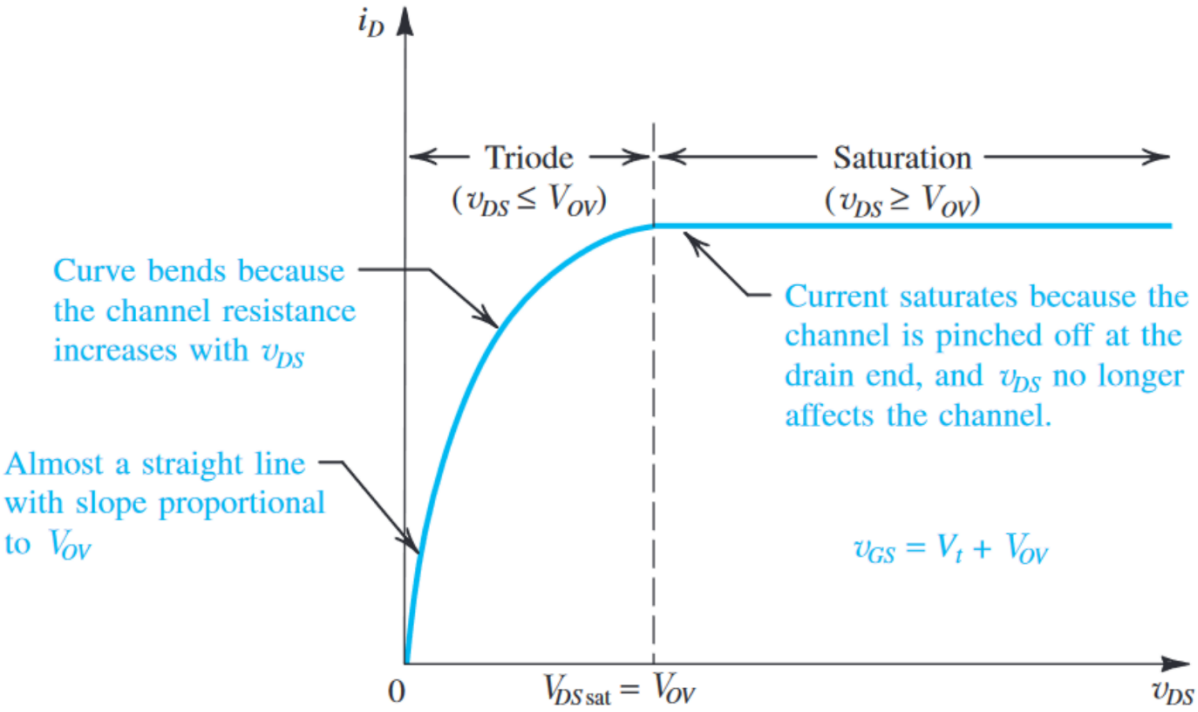


Figure 7: The drain current I_D versus the drain-to-source voltage V_{DS} for an enhancement-type NMOS transistor operated with $V_{GS} = V_{th} + V_{OV}$.

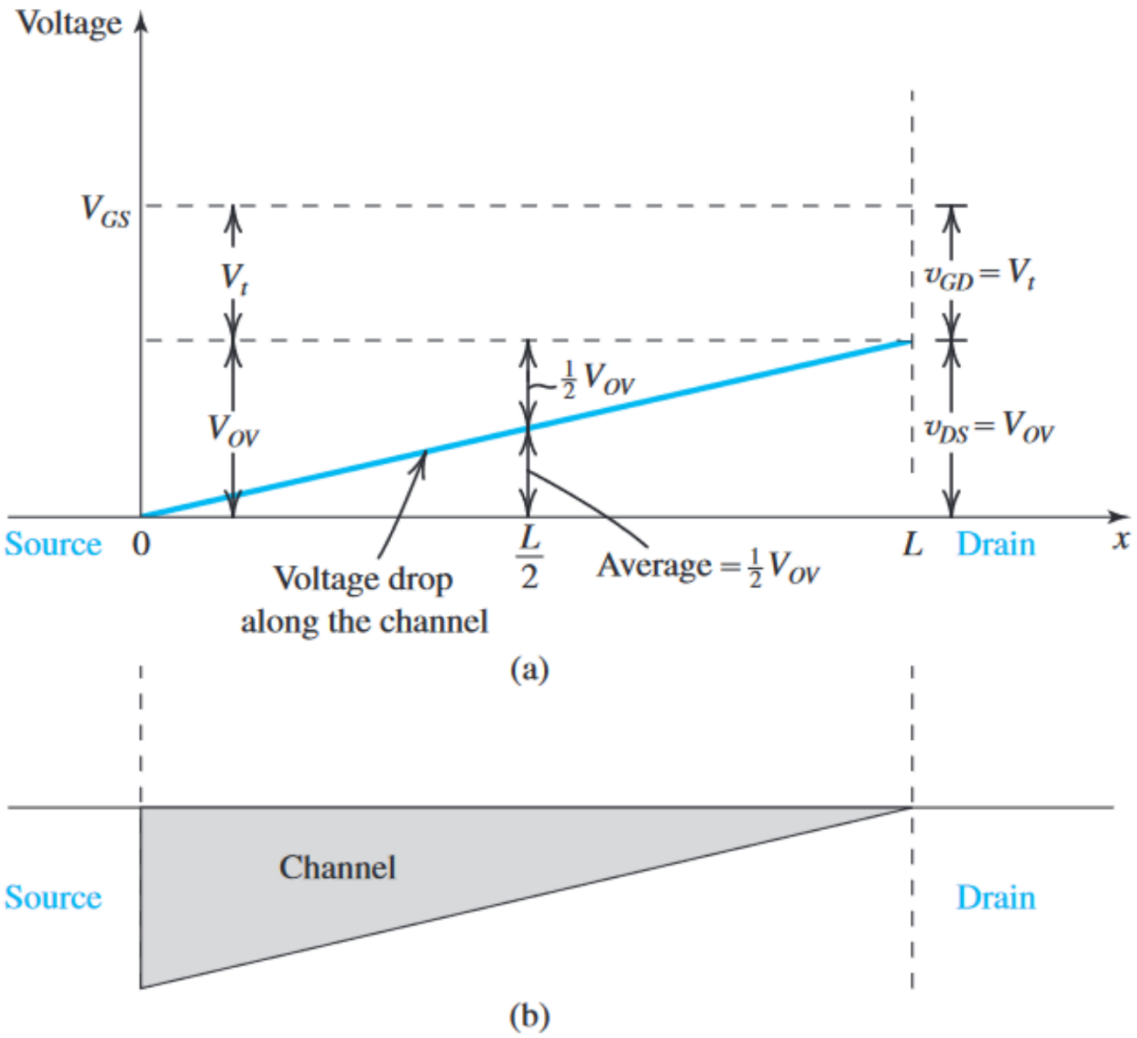


Figure 8: Operation of MOSFET with $V_{GS} = V_{th} + V_{OV}$, as V_{DS} is increased to V_{OV}. At the drain end, V_{GD} decreases to V_{th} and the channel depth at the drain end reduces to zero (pinch-off). At this point, the MOSFET enters the saturation mode of operation. Further increasing V_{DS} (beyond $V_{DSsat} = V_{OV}$) has no effect on the channel shape and I_D remains constant.

Exercice 2

Consider a process technology for which L_{min} = 0.4 µm, t_{ox} = 8 nm, μ_n = 450 cm^2 /V·s, and V_{th} = 0.7 V.

(a) Find C*ox* and k′$_n$.

(b) For a MOSFET with W/L = 8 µm/0.8 µm, Calculate the values of V_{OV}, V_{GS}, and V_{DSmin} needed to operate the transistor in the saturation region with a dc current I_D = 100µA.

(c) For the device in (b), find the values of V_{OV} and V_{GS} required to cause the device to operate as a 1000 Ω-resistor for very small V_{DS}.

Answers: (a) 4.32 fF/μm^2. 194 $\mu A/V^2$.

(b) 0.32 V. 1.02 V. 0.32 V.

(c) 0.52 V. 1.22 V.
