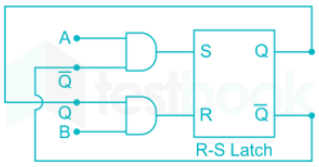
Sequential circuits Tutorial Session – 2

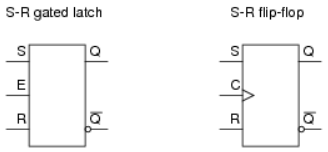
1. SR Latch:

The two inputs A and B are connected to a NOR based SR latch, via two AND gates as shown in the figure.
If A = 1 and B= 1, give the values of the output Q and Q.



2. SR Latch:

Plain S-R latch circuits are "set" by activating the S input and de-activating the R input. Conversely, they are "reset" by activating the R input and de-activating the S input. Gated latches and flip-flops, however, are a little more complex:

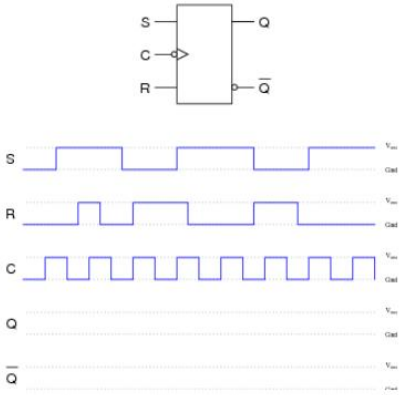


Describe what input conditions have to be present to force each of these multivibrator circuits to *set* and to *reset*.

For the S-R gated latch:	For the S-R flip-flop:
Set by . . .	Set by . . .
Reset by . . .	Reset by . . .

3. SR Latch:

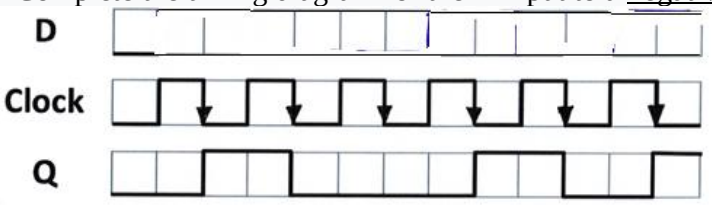
Determine the output states for this S-R flip-flop, given the pulse inputs shown:



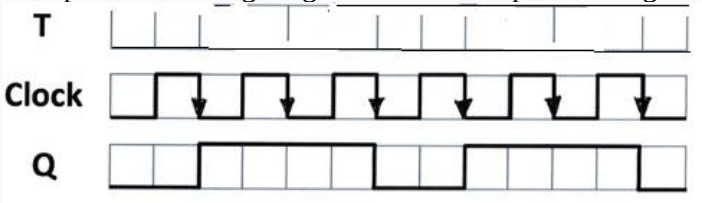
4. Flip-Flop and Timing Diagrams:

Complete the timing diagram for the specified flip-flop such the output Q will be as indicated. Assume that the input signal can change only on the vertical lines. Also, assume that the setup time t_{su} and the hold time t_h are each equal to the width of one square.

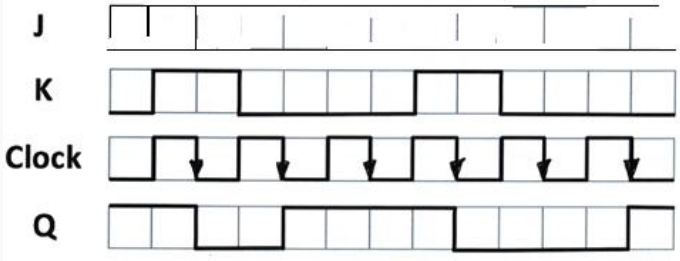
a- Complete the timing diagram for the D input to a negative-edge triggered D flip-flop.



b- Complete the timing diagram for the T input to a negative-edge triggered T flip-flop.



c- Complete the timing diagram for the J input to a negative-edge triggered JK flip-flop.

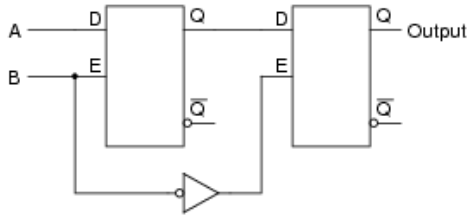


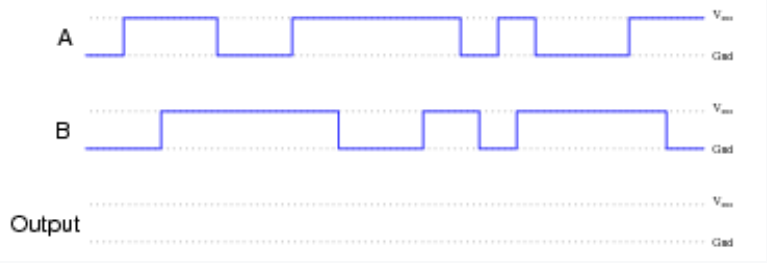
5. D Latch:

Determine the final output states over time for the following circuit, built from D-type gated latches:

At what specific times in the pulse diagram does the final output assume the input's state?

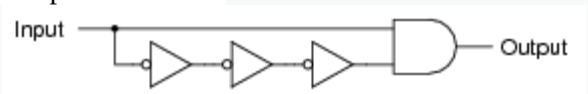
How does this behavior differ from the normal response of a D-type latch?





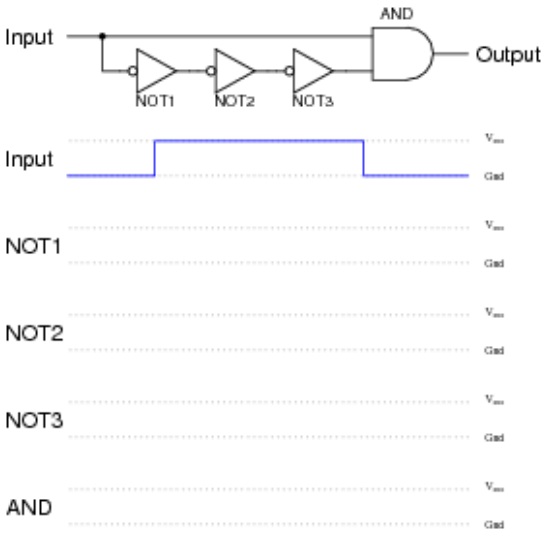
6. Propagation delay of logic gates:

Usually, propagation delay is considered an undesirable characteristic of logic gates, which we simply have to live with. Other times, it is a useful, even necessary, trait. Take for example this circuit:



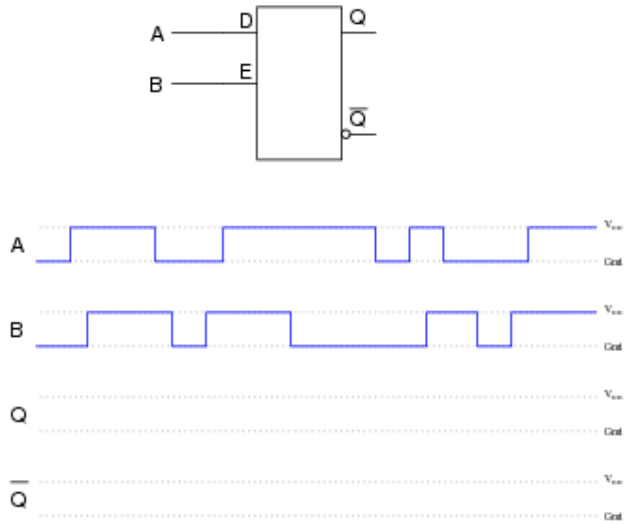
If the gates constituting this circuit had zero propagation delay, it would perform no useful function at all. To verify this sad fact, analyze its steady-state response to a "low" input signal, then to a "high" input signal. What state is the AND gate's output always in?

Now, consider propagation delay in your analysis by completing a timing diagram for each gate's output, as the input signal transitions from low to high, then from high to low:



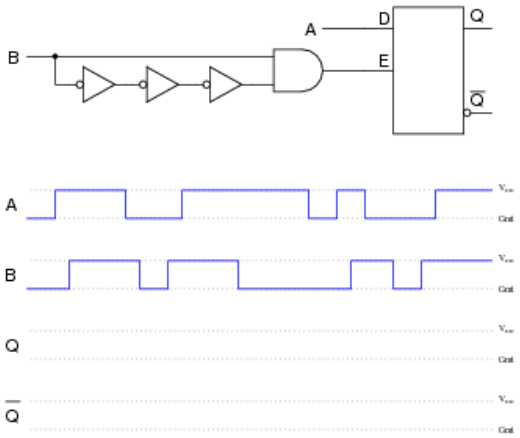
7. D Latch & Propagation delay of logic gates:

a- Determine the Q and Q output states of this D-type gated latch, given the following input conditions:



Determine the Q and Q output states of this D-type gated latch, given the following input conditions:

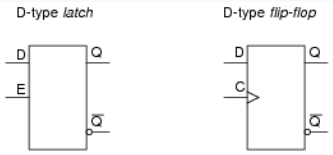
b- Now, suppose we add a propagation-delay-based one-shot circuit to the Enable line of this D-type gated latch. Re-analyze the output of the circuit, given the same input conditions:



Comment on the differences between these two circuits' responses, especially with reference to the enabling input signal (B).

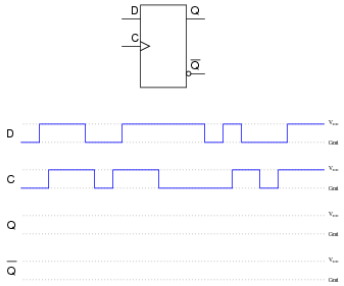
8. D Latch:

Shown here are two digital components: a D-type *latch* and a D-type *flip-flop*:
Other than the silly name, what distinguishes a "flip-flop" from a latch? How do the two circuits differ in function?



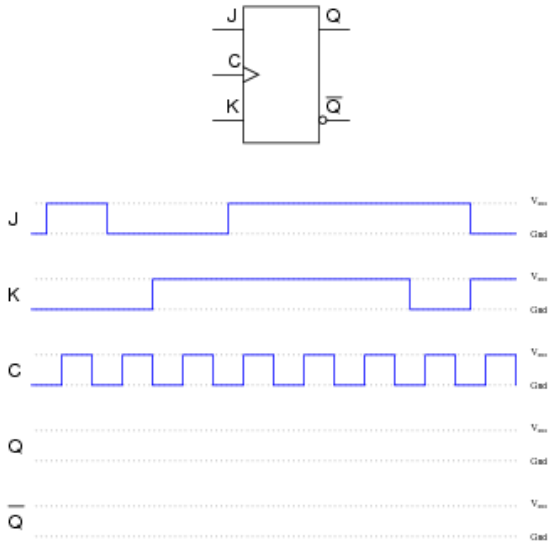
9. D flip-flop:

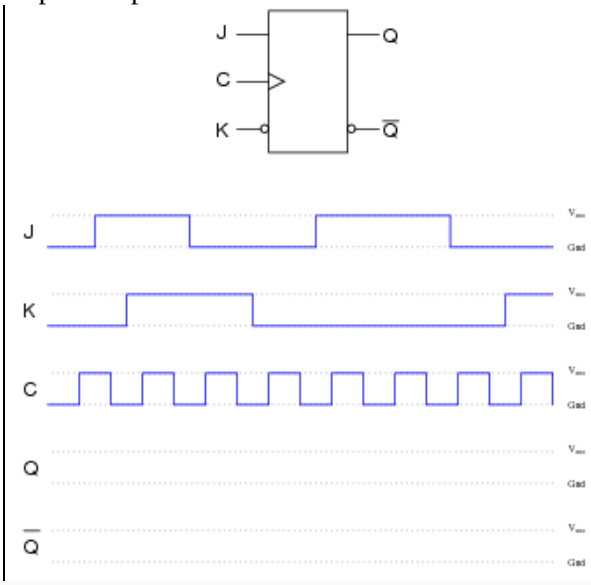
Determine the output states for this D flip-flop, given the pulse inputs shown:



10. JK Flip-Flop:

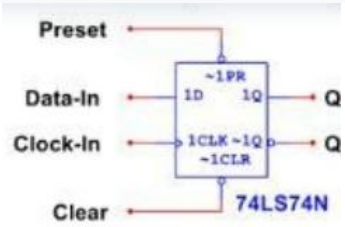
Determine the output states for these J-K flip-flops, given the pulse inputs shown:





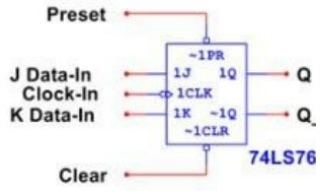
11. D flip-flop:

For the 74LS74 **D flip-flop** shown in the following figure, complete the timing diagram for the output signal **Q**. **Note** that the **CLK** input (clock) for this flip-flop is a positive edge **trigger** and both the **PR** and **CLR** asynchronous inputs (Preset and Clear) are active low.



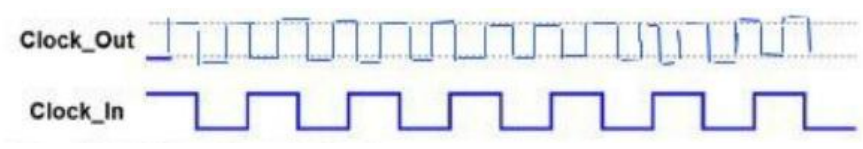
12. JK Flip-Flop:

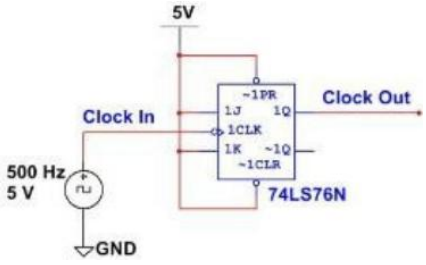
For the 74LS76 **JK flip-flop** shown in the following figure, complete the timing diagram for the output signal **Q**. **Note** that the **CLK** input for this flip-flop is a negative edge **trigger** and both the **PR** and **CLR** asynchronous inputs (Preset and Clear) are active low.



13. JK Flip-Flop as a divide-by-two circuit:

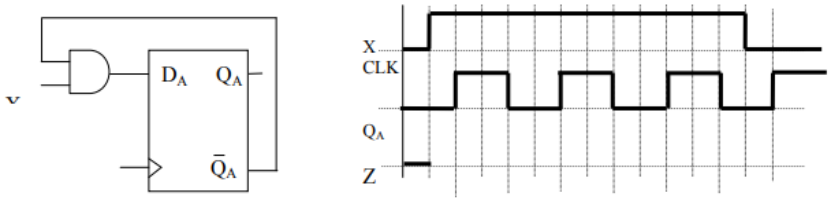
A divider-by-two circuit is implemented with a JK flip-flop.
It generates a clock output that is half the frequency of the clock input.
Predict the timing diagram for a **JK** Divider-by-two circuit.





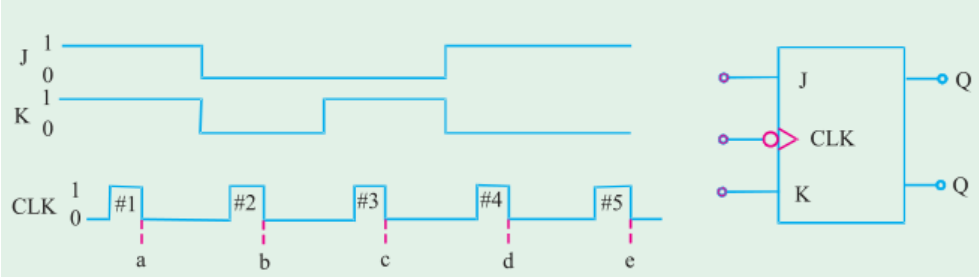
14. D Flip-Flop:

For the sequential circuit below, draw the waveform of the output (Q_A).

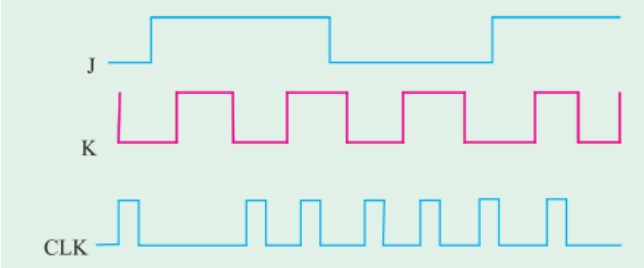


15. JK Flip-Flop:

The following figure shows the waveforms applied at J, K and CLK inputs of the clocked J-K flip-flop. Sketch the Q output waveform Assume Q = 0 initially.

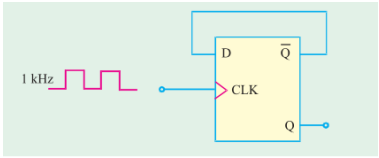


What will be the output waveform Q of a J-K flip-flop if the following waveforms are applied at the input? Assume the flip-flop triggers at the falling edge of clock pulse.



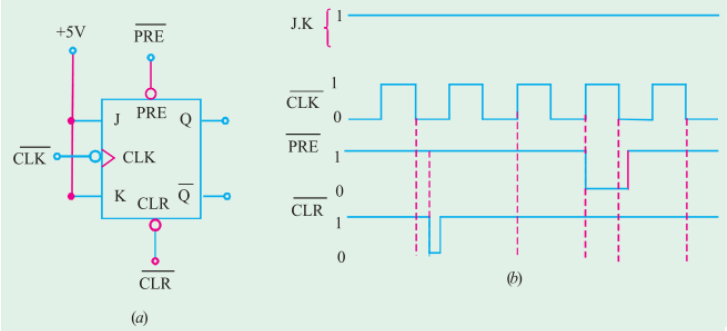
16. D Flip-Flop:

An edge-triggered D Flip-flop can be made to operate in the toggle mode by connecting it as shown below.
Assume Q = 0 initially and determine the Q (output) waveform.

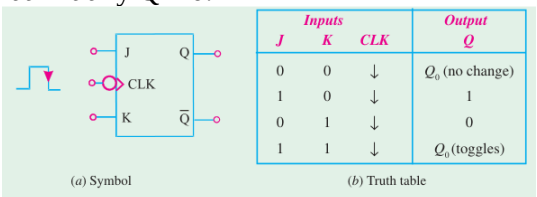


17. Clocked J-K Flip-Flop with Asynchronous Inputs:

The following figure (a) shows the logic symbol for a J-K flip-flop that responds to the falling edge on its clock pulse and has active-LOW asynchronous inputs. The J and K inputs are tied HIGH.



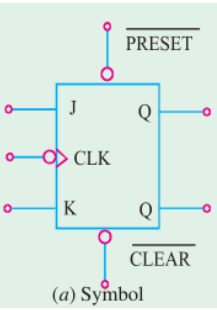
Using the following true table, determine the Q-output in response to the waveforms shown in Fig. (b). Assume that initially Q = 0.



Inputs J	Inputs K	Inputs CLK	Output Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	Q_0 (toggles)

(b) Truth table

Fig. Falling edge triggered J-K flip-flop.



Inputs $\overline{PRESET}$	Inputs $\overline{CLEAR}$	Output / Flip-flop response
1	1	Clocked operation*
0	1	Q = 1 (regardless of CLK)
1	0	Q = 0 (regardless of CLK)
0	0	Not used

(b) Truth table