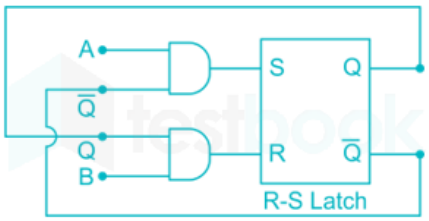
Sequential circuits Tutorial Session – 2 (with Answers)

1. SR Latch:

The two inputs A and B are connected to a NOR based SR latch, via two AND gates as shown in the figure.
If A = 1 and B= 1, give the values of the output Q and Q.



Answer 1:

From the given diagram,

$S = A\bar{Q}$, $R = QB$

Given that, A = 1, B = 0

$S = \bar{Q}$, $R = 0$

The truth table of the S-R latch is:

S	R	Q_{n+1}
0	0	No Change
0	1	0
1	0	1
1	1	Invalid state

Let Q = 0,

$S = \bar{Q} = 1$, $R = 0 \Rightarrow Q_{n+1} = 1$

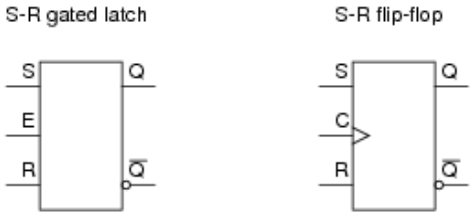
Let Q = 1,

$S = \bar{Q} = 0$, $R = 0 \Rightarrow Q_{n+1} = 1$

In both the cases, $Q_{n+1}\,\bar{Q}_{n+1} = 10$

2. SR Latch:

Plain S-R latch circuits are "set" by activating the S input and de-activating the R input. Conversely, they are "reset" by activating the R input and de-activating the S input. Gated latches and flip-flops, however, are a little more complex:



Describe what input conditions have to be present to force each of these multivibrator circuits to *set* and to *reset*.

For the S-R gated latch:

Set by . . .
Reset by . . .

For the S-R flip-flop:

Set by . . .
Reset by . . .

Answer 2:

For the S-R gated latch:

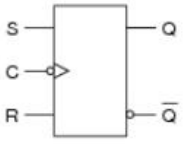
Set by making S high, R low, and E high.
Reset by making R high, S low, and E high.

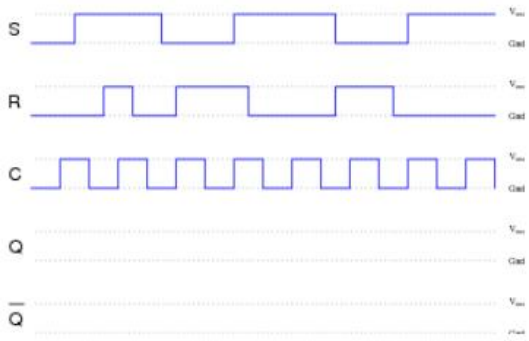
For the S-R flip-flop:

Set by making S high, R low, and C transition from low to high.
Reset by making R high, S low, and C transition from low to high.

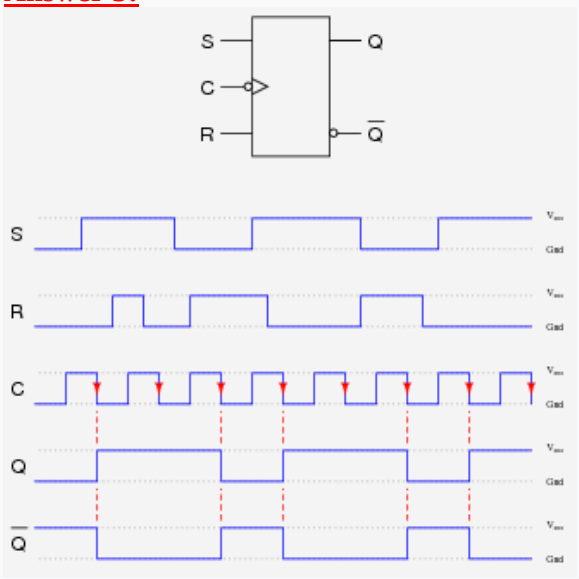
3. SR Latch:

Determine the output states for this S-R flip-flop, given the pulse inputs shown:





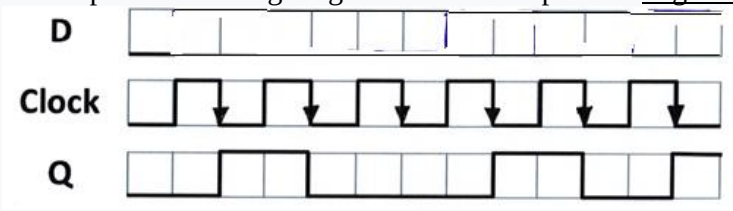
Answer 3:



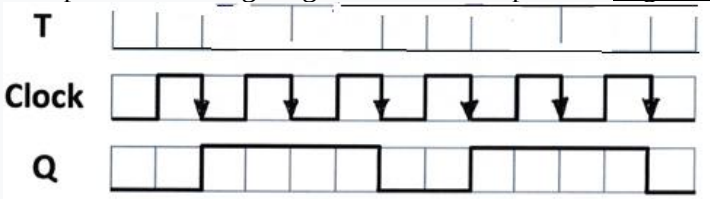
4. Flip-Flop and Timing Diagrams:

Complete the timing diagram for the specified flip-flop such the output Q will be as indicated. Assume that the input signal can change only on the vertical lines. Also, assume that the setup time t_{su} and the hold time t_h are each equal to the width of one square.

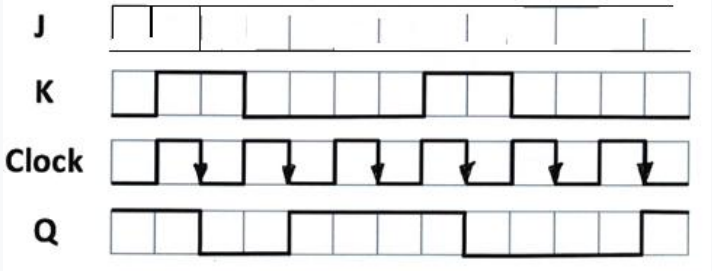
a- Complete the timing diagram for the D input to a negative-edge triggered D flip-flop.



b- Complete the timing diagram for the T input to a negative-edge triggered T flip-flop.

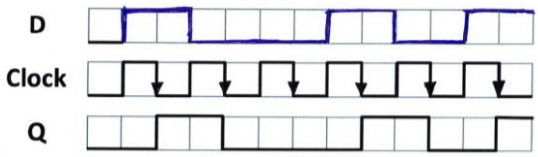


c- Complete the timing diagram for the J input to a negative-edge triggered JK flip-flop.

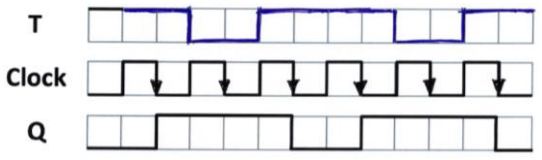


Answer 4:

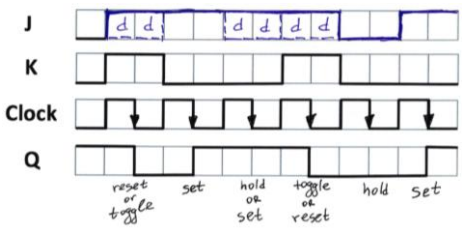
a-



b-

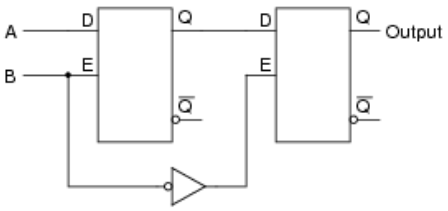


c-



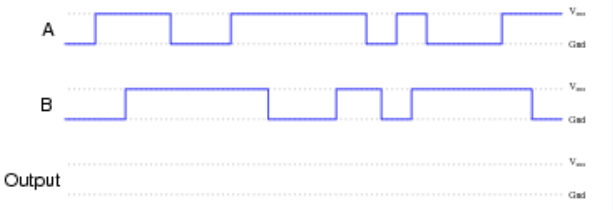
5. D Latch:

Determine the final output states over time for the following circuit, built from D-type gated latches:



At what specific times in the pulse diagram does the final output assume the input's state?

How does this behavior differ from the normal response of a D-type latch?

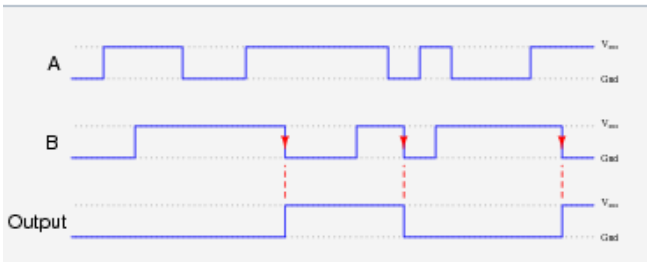


Answer 5:

The final output assumes the same logic state as the input only when the enable input signal (B) *transitions* from "high" to "low".

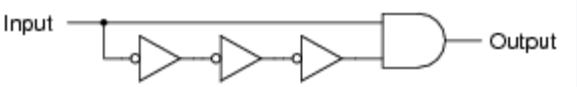
Notes:

Note that by adding another latch, the overall behavior only slightly resembles the behavior of a D-type latch. With the addition of the second latch, we've changed this circuit into a *flip-flop*, specifically of the *master-slave* variety.



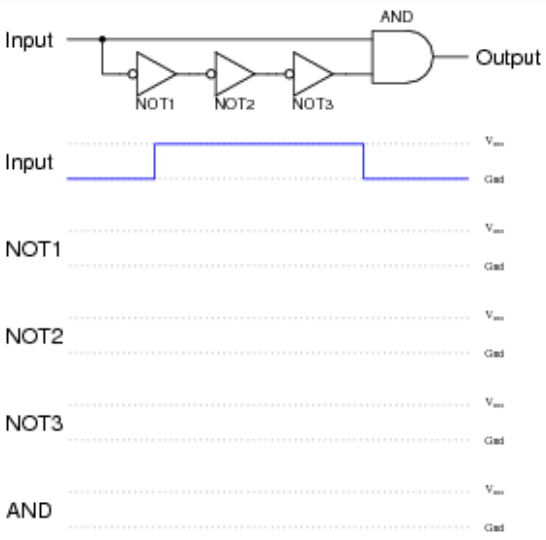
6. Propagation delay of logic gates:

Usually, propagation delay is considered an undesirable characteristic of logic gates, which we simply have to live with. Other times, it is a useful, even necessary, trait. Take for example this circuit:



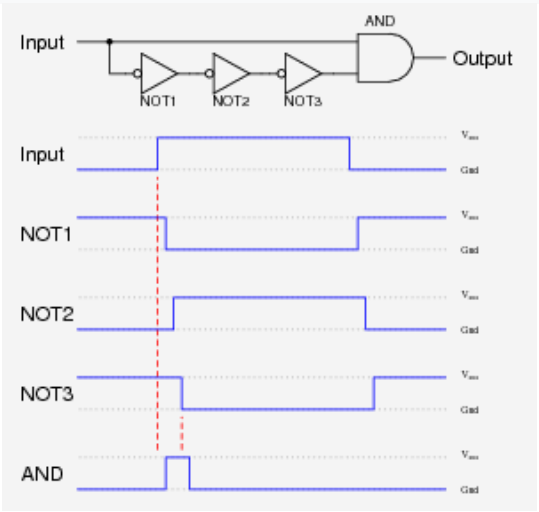
If the gates constituting this circuit had zero propagation delay, it would perform no useful function at all. To verify this sad fact, analyze its steady-state response to a "low" input signal, then to a "high" input signal. What state is the AND gate's output always in?

Now, consider propagation delay in your analysis by completing a timing diagram for each gate's output, as the input signal transitions from low to high, then from high to low:



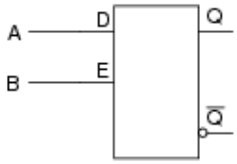
Answer 6:

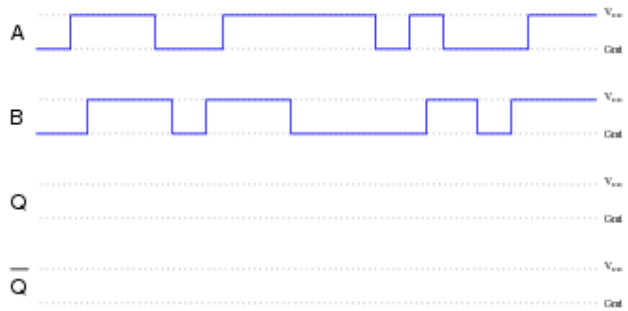
Follow-up question: describe exactly what conditions are necessary to obtain a "high" signal from the output of this circuit, and what determines the duration of this "high" pulse. This circuit is a special type of *one-shot*, outputting a single pulse of limited duration for each leading-edge transition of the input signal.



7. D Latch & Propagation delay of logic gates:

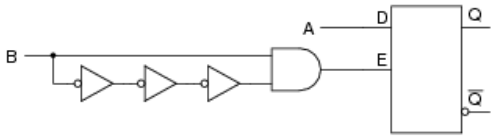
a- Determine the Q and Q output states of this D-type gated latch, given the following input conditions:

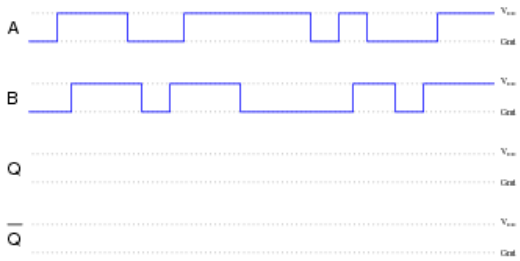




Determine the Q and Q output states of this D-type gated latch, given the following input conditions:

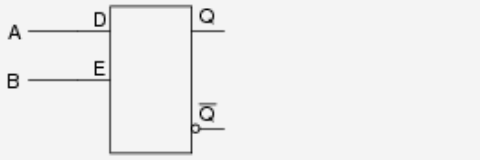
b- Now, suppose we add a propagation-delay-based one-shot circuit to the Enable line of this D-type gated latch. Re-analyze the output of the circuit, given the same input conditions:

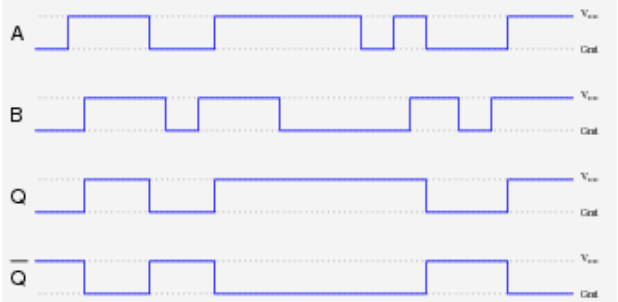


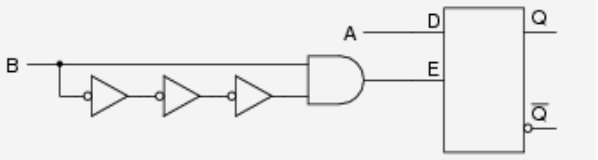


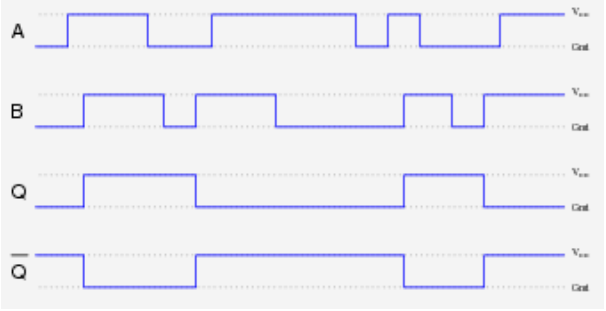
Comment on the differences between these two circuits' responses, especially with reference to the enabling input signal (B).

Answer 7:









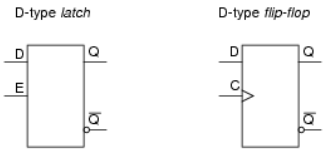
Follow-up question: one of these circuits is referred to as *edge-triggered*. Which one is it?

Challenge question: in reality, the output waveforms for both these scenarios will be shifted slightly due to propagation delays within the constituent gates. Re-draw the true outputs, accounting for these delays.

8. D Latch:

Shown here are two digital components: a D-type *latch* and a D-type *flip-flop*:

Other than the silly name, what distinguishes a "flip-flop" from a latch? How do the two circuits differ in function?

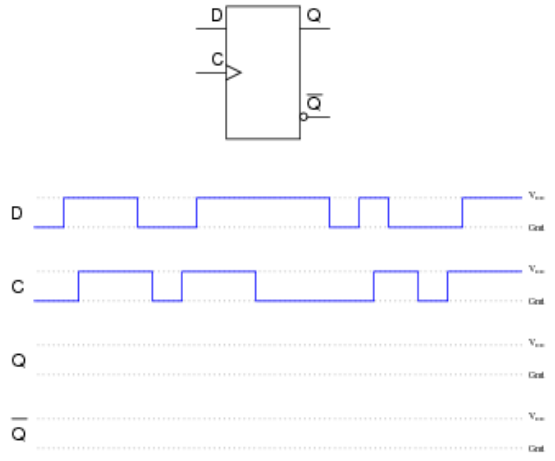


Answer 8:

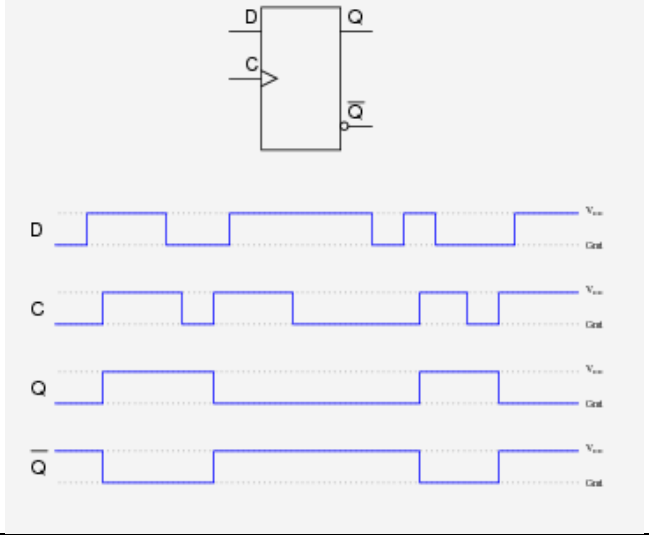
A "flip-flop" is a latch that changes output only at the rising or falling *edge* of the clock pulse.

9. D flip-flop:

Determine the output states for this D flip-flop, given the pulse inputs shown:

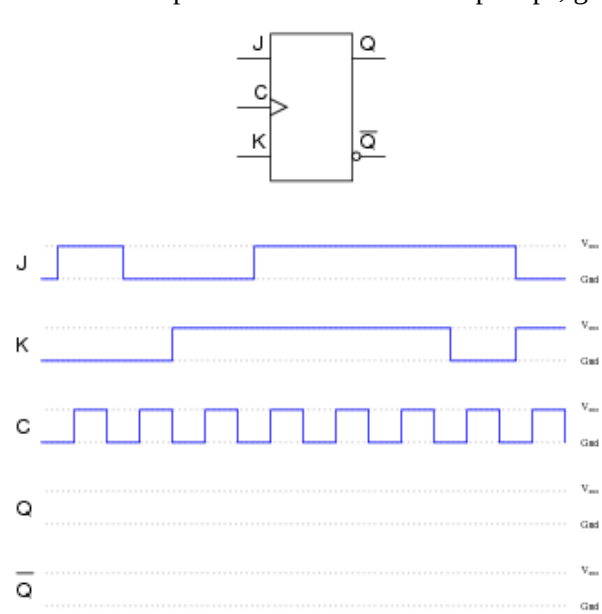


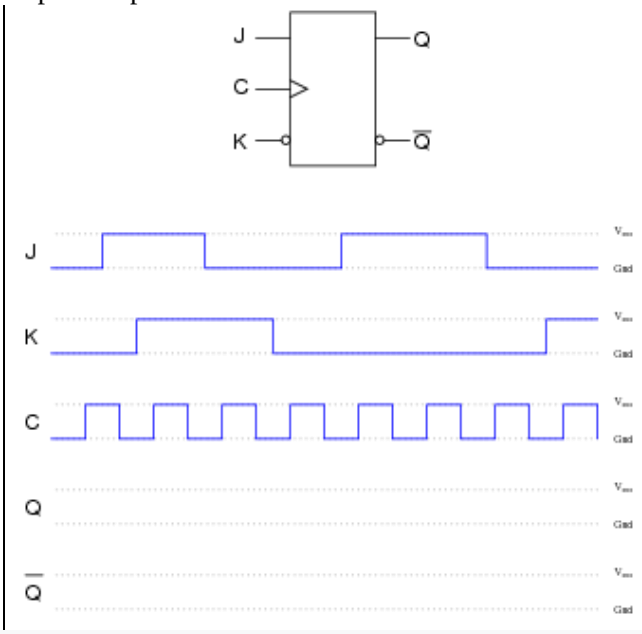
Answer 9:



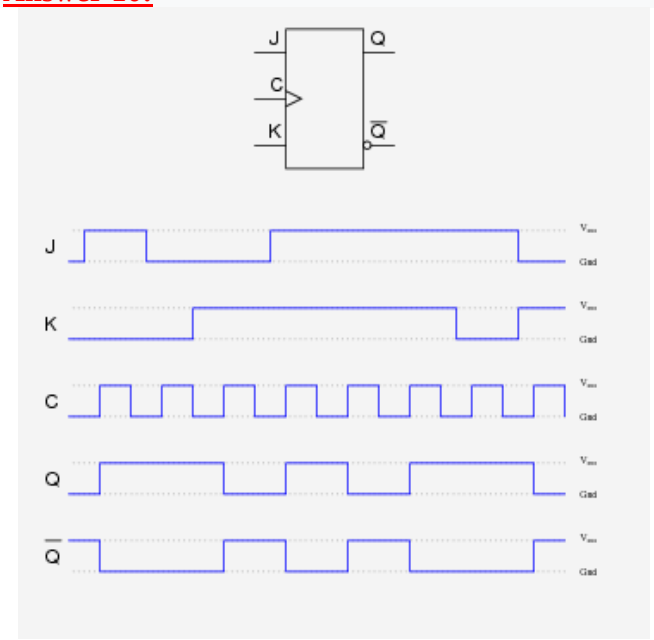
10. JK Flip-Flop:

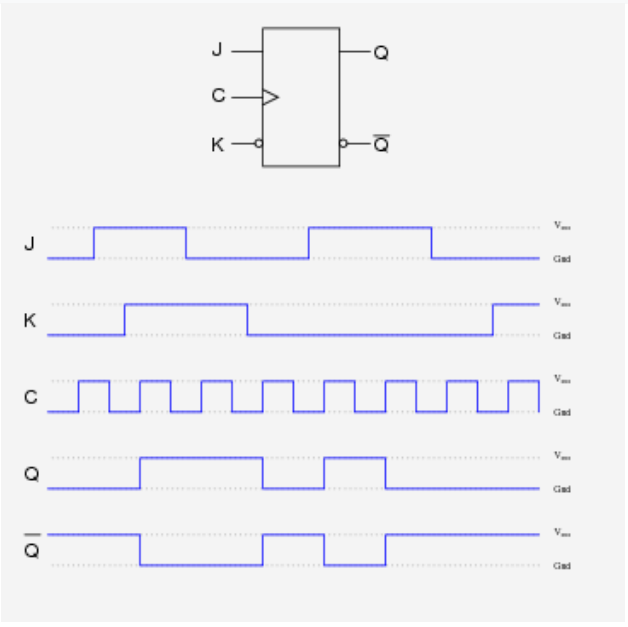
Determine the output states for these J-K flip-flops, given the pulse inputs shown:





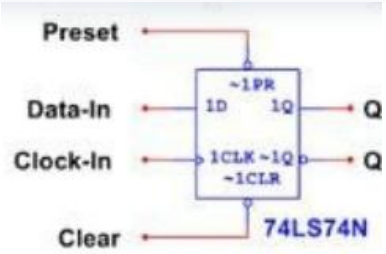
Answer 10:



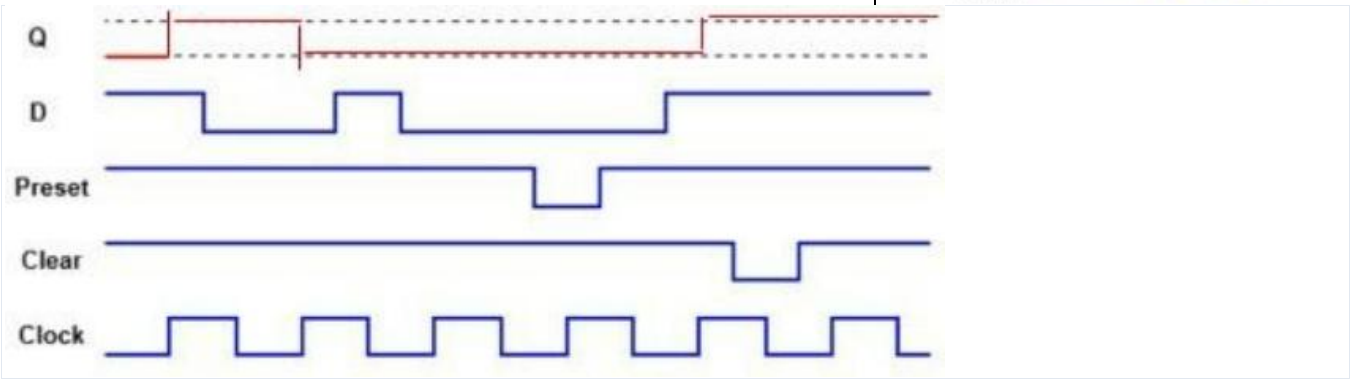


11. D flip-flop:

For the 74LS74 **D flip-flop** shown in the following figure, complete the timing diagram for the output signal **Q**. **Note** that the **CLK** input (clock) for this flip-flop is a positive edge **trigger** and both the **PR** and **CLR** asynchronous inputs (Preset and Clear) are active low.

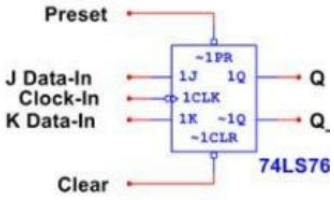


Answer 11:

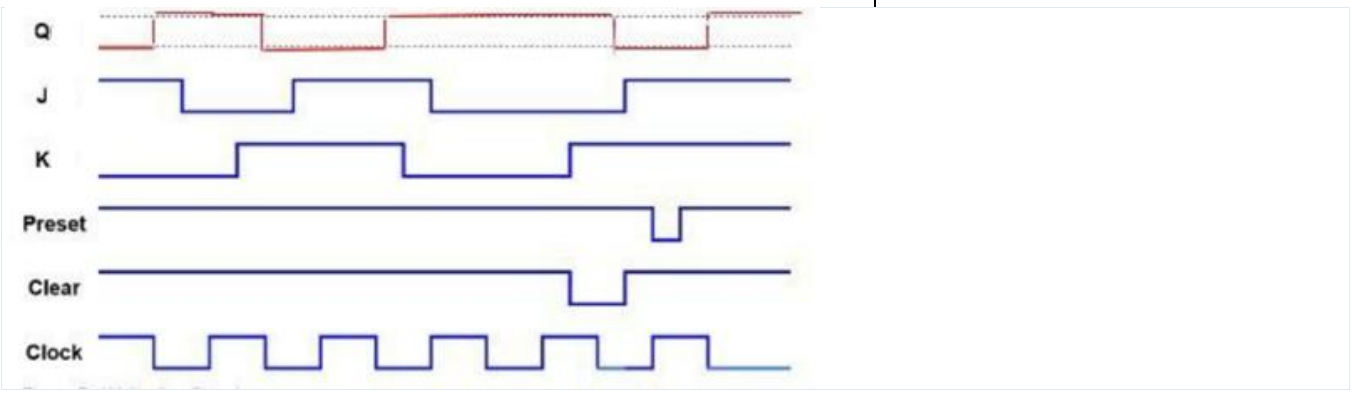


12. JK Flip-Flop:

For the 74LS76 **JK flip-flop** shown in the following figure, complete the timing diagram for the output signal **Q**. **Note** that the **CLK** input for this flip-flop is a negative edge **trigger** and both the **PR** and **CLR** asynchronous inputs (Preset and Clear) are active low.

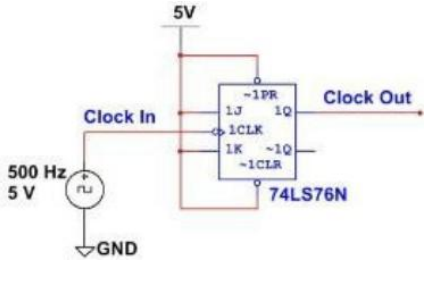


Answer 12:

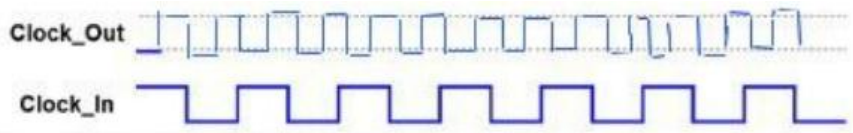


13. JK Flip-Flop as a divide-by-two circuit:

A divider-by-two circuit is implemented with a JK flip-flop.
It generates a clock output that is half the frequency of the clock input.
Predict the timing diagram for a **JK** Divider-by-two circuit.

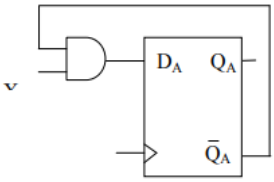


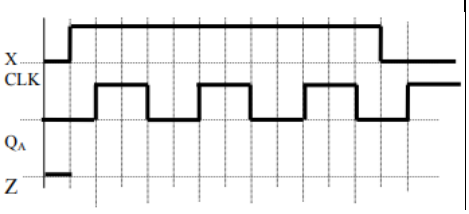
Answer 13:



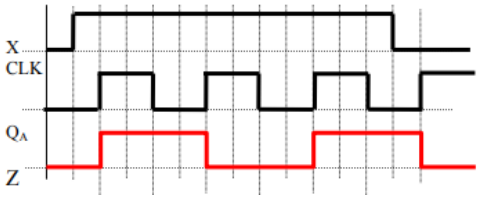
14. D Flip-Flop:

For the sequential circuit below, draw the waveform of the output (Q_A).



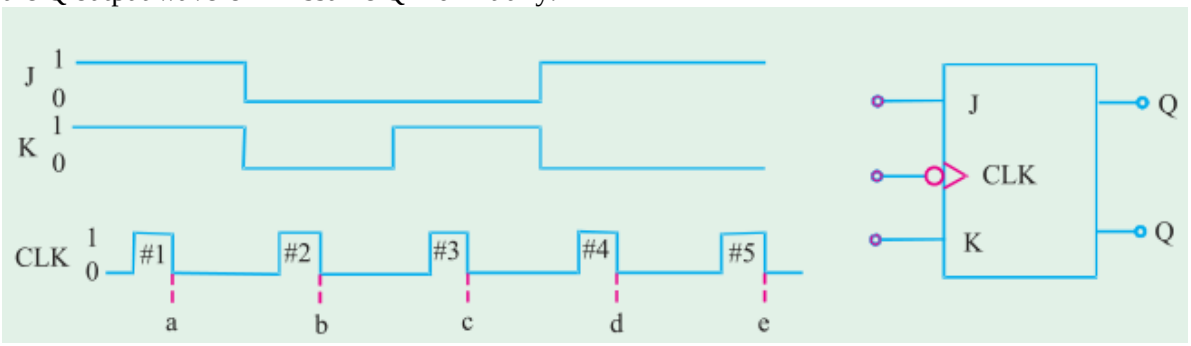


Answer 14:

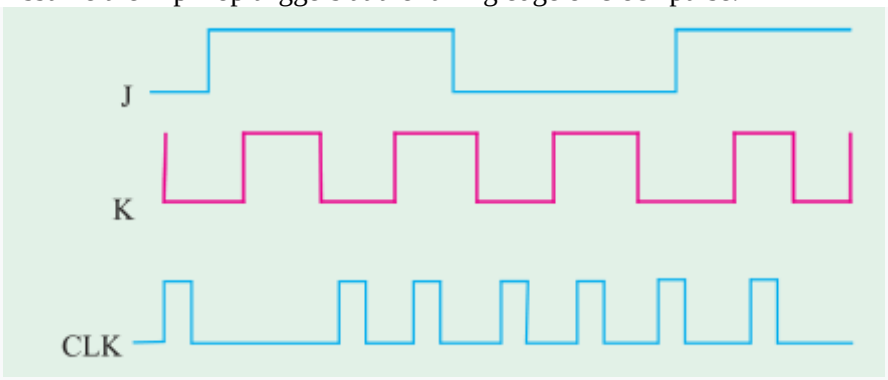


15. JK Flip-Flop:

The following figure shows the waveforms applied at J, K and CLK inputs of the clocked J-K flip-flop. Sketch the Q output waveform Assume Q = 0 initially.

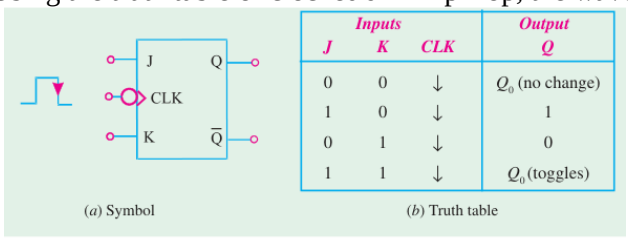


What will be the output waveform Q of a J-K flip-flop if the following waveforms are applied at the input? Assume the flip-flop triggers at the falling edge of clock pulse.



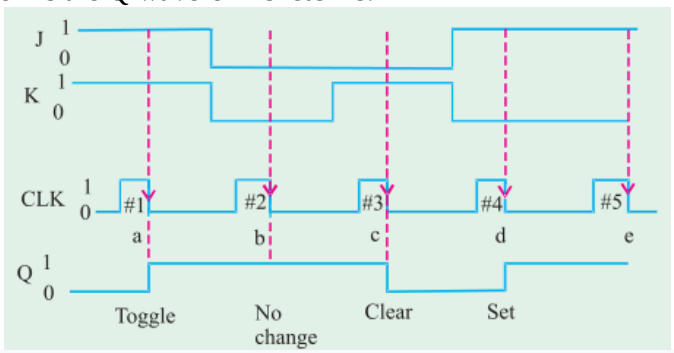
Answer 15:

Using the truth table of clocked J-K flip-flop, the waveforms the Q-waveform sketch is:

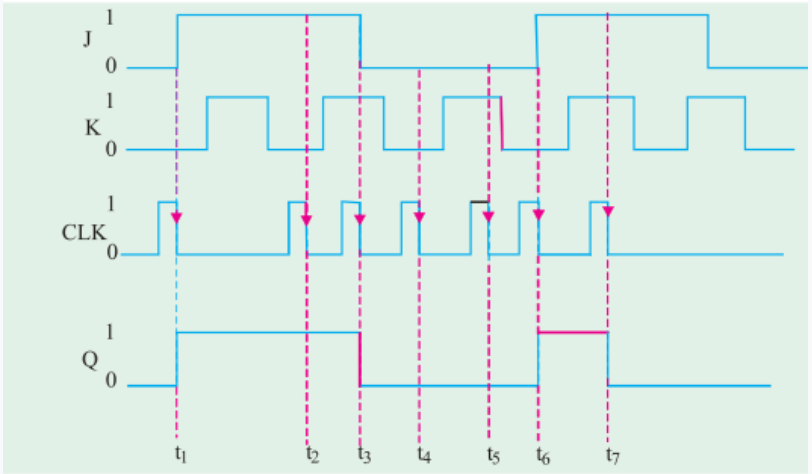


Inputs J	K	CLK	Output Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	Q_0 (toggles)

Fig. Falling edge triggered J-K flip-flop.

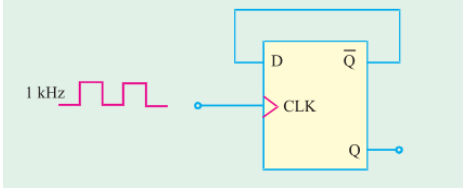


Recall the truth table of a clocked J-K flip-flop, We can sketch the Q-output waveform as shown in Fig:



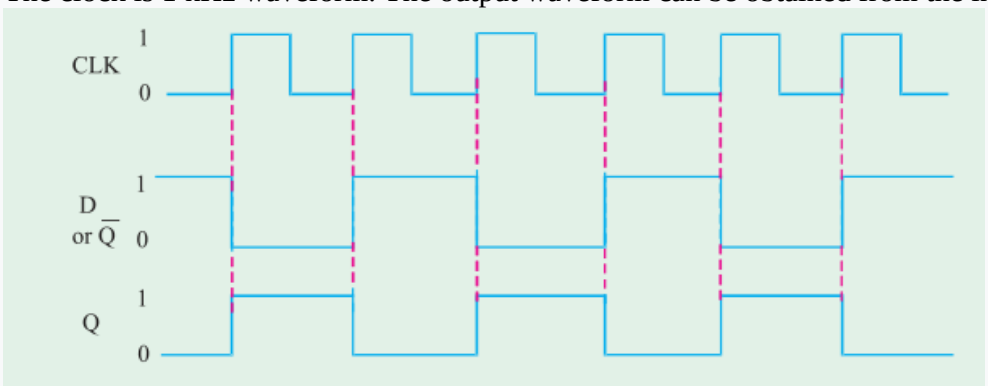
16. D Flip-Flop:

An edge-triggered D Flip-flop can be made to operate in the toggle mode by connecting it as shown below.
Assume Q = 0 initially and determine the Q (output) waveform.



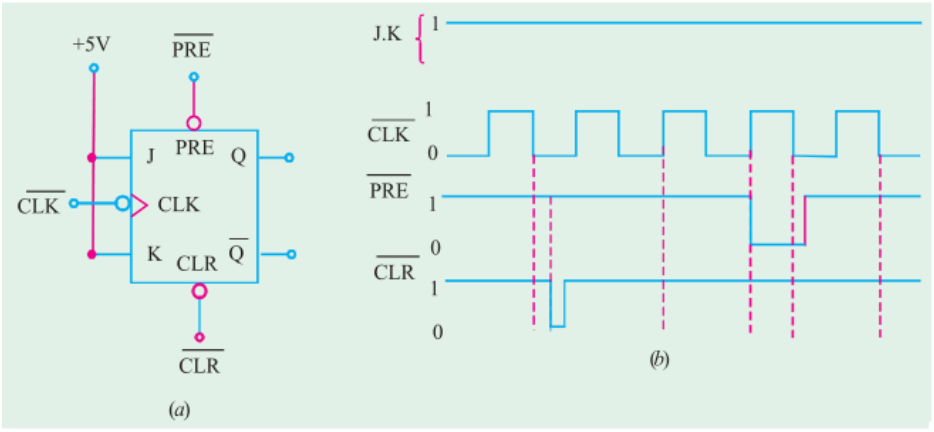
Answer 16:

The clock is 1 kHz waveform. The output waveform can be obtained from the input as shown in Fig.

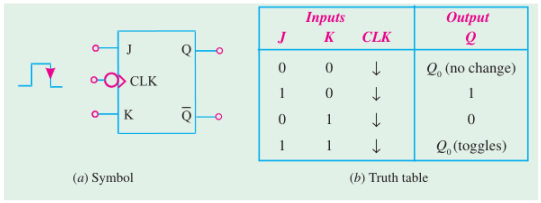


17. Clocked J-K Flip-Flop with Asynchronous Inputs:

The following figure shows the logic symbol for a J-K flip-flop that responds to the falling edge on its clock pulse and has active-LOW asynchronous inputs. The J and K inputs are tied HIGH.

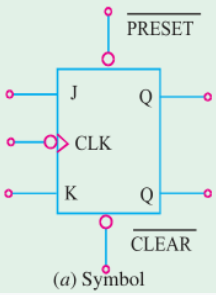


Using the following true tables, determine the Q-output in response to the waveforms shown in Fig. (b). Assume that initially Q = 0.



Inputs			Output
J	*K*	*CLK*	*Q*
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	Q_0 (toggles)

Fig. Falling edge triggered J-K flip-flop.



Inputs		Output / Flip-flop response
$\overline{PRESET}$	$\overline{CLEAR}$	
1	1	Clocked operation*
0	1	Q = 1 (regardless of CLK)
1	0	Q = 0 (regardless of CLK)
0	0	Not used

(b) Truth table

Answer 17:

In order to sketch the Q-output waveform, recall the truth tables of J-K flip-flop