Exercise 01

Let's assume signed 8-bit numbers. Under which conditions do the following additions change the CY flag, and specify if there is an overflow:

- Positive Number + Positive Number
- Positive Number + Negative Number
- Negative Number + Negative Number

Exercise 02

Let's assume that the ALU accepts two inputs, X and Y, each composed of 8 bits (X_7 to X_0 and Y_7 to Y_0). Assume that the output of the ALU is T, also 8 bits (T_7 to T_0). Finally, suppose that T_8 is available and acts as an additional bit for the ALU result (adding two 8-bit values may result in a 9-bit output). Design a logic circuit that generates the S, CY, AC, Z, and P flags based on the bits of the inputs and outputs during a two's complement addition.

Exercise 03

If A and B are strictly positive, which instruction should be used, and which flag should be checked to determine if:

- A is equal to B ? A is greater than B ? A is greater than or equal to B ? A is less than B ? A is less than or equal to B ?

Exercise 04

The accumulator A is represented by the eight bits (A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0). Which instruction should be used to mask (set to 0) the two bits A_6 and A_5 without modifying the other bits ? And to set them to 1 ?

Exercise 05

Specify the addressing modes of each of the following instructions: MVI A,41H - CMA - MOV C,B - LXI H,1234H - DCR A - SUB D - MOV E,M - SUB M - ADI 78H - RLC - SPHL - STA 0400H - MVI M,10H - JMP 3000H - STAX B - IN 05H - CALL 4000H - RET