

FLIP-FLOPS

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FlipFlop

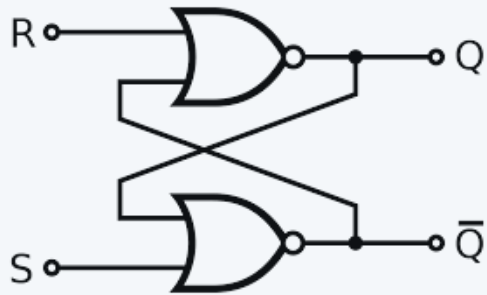
- The memory elements used in clocked sequential circuits are called flipflops. These circuits are binary cells capable of storing one bit of information.
- A flipflop circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit)until directed by an input signal to switch states
- A bi stable device
- Have two outputs one complement of another
- Applications of Flipflops
 - ▣ Counters
 - ▣ Shift Registers
 - ▣ Storage Registers
 - ▣ Frequency Dividers

Basic Flipflop (RS Latch)

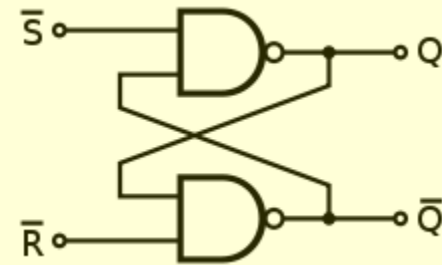
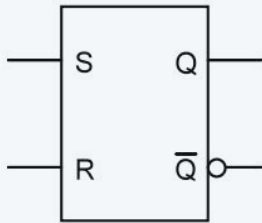
- The **SR flip-flop**, also known as a *SR Latch*, can be considered as one of the most basic sequential logic circuit possible.
- This simple flip-flop is basically a one-bit memory bistable device that has two inputs, one which will “SET” the device (meaning the output = “1”), and is labelled **S** and one which will “RESET” the device (meaning the output = “0”), labelled **R**.
- SR stands for “Set-Reset”.
- The reset input resets the flip-flop back to its original state with an output Q that will be either at a logic level “1” or logic “0” depending upon this set/reset condition.

Basic Flipflop (RS latch)

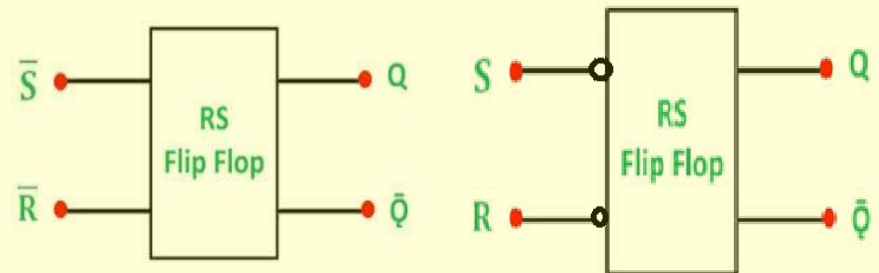
- Basic Flipflop can be constructed using two NAND gates or using two NOR gates
- **[Set means $Q=1$, $Q'=0$ and Reset means $Q=0$, $Q'=1$]**



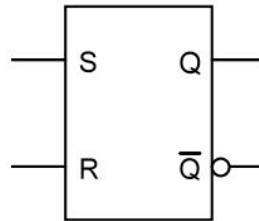
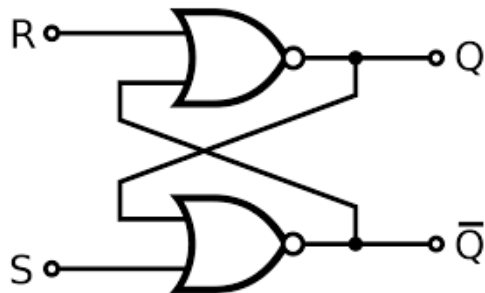
Active High



Active Low



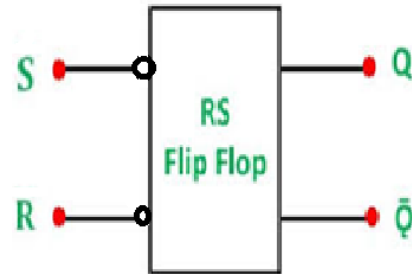
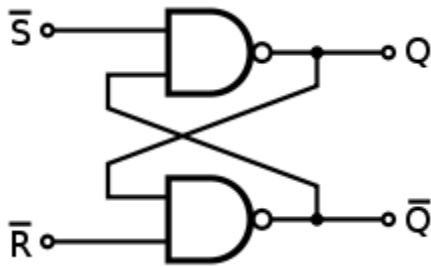
Active High



S	R	Q	Q'	
1	0	1	0	set
0	0	1	0	No change
0	1	0	1	Reset
0	0	0	1	No change
1	1	?	?	Undefined

- Under normal operation, both inputs remain at 0 unless the state of Flipflop has to be changed
- The application of momentary 1 to the Set input (S) causes flipflop to go to set state ($Q=1, Q'=0$).
- The set input goes back to 0.
- A momentary 1 applied to the reset input causes the flipflop to go to Reset state ($Q=0, Q'=1$)
- Both inputs at 0 leaves the state of flipflop unchanged
- Applying 1 at both inputs gives rise to undefined state and must be avoided.

Active Low

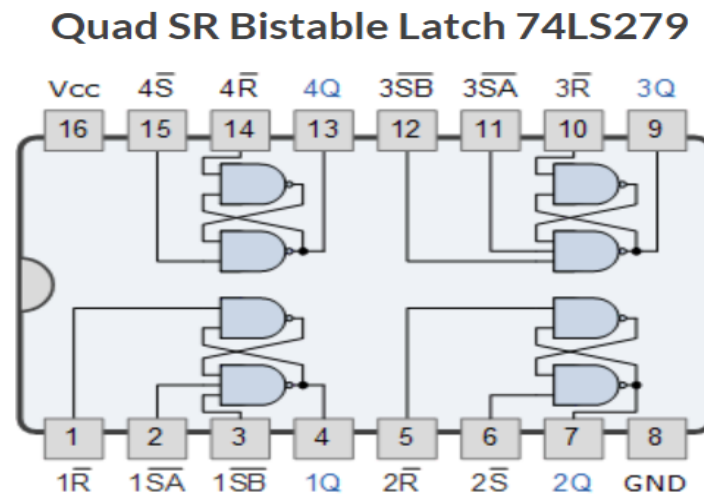


S	R	Q	Q'	
0	1	1	0	set
1	1	1	0	No change
1	0	0	1	Reset
1	1	0	1	No change
0	0	?	?	Undefined

- Under normal operation, both inputs remain at 1 unless the state of Flipflop has to be changed
- The application of momentary 0 to the Set input (S) causes flipflop to go to set state ($Q=1$, $Q'=0$).
- The set input goes back to 1.
- A momentary 0 applied to the reset input causes the flipflop to go to Reset state ($Q=0$, $Q'=1$)
- Both inputs at 1 leaves the state of flipflop unchanged
- Applying 0 at both inputs gives rise to undefined state and must be avoided.

RS flipflop IC (Active Low)

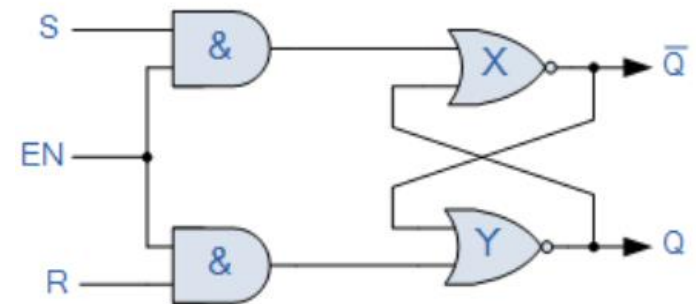
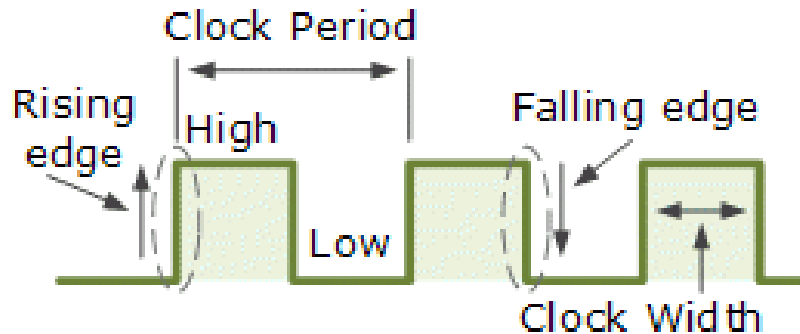
The 74LS279 is a Quad SR Bistable Latch IC, which contains four individual NAND type (Active Low) Flipflop within a single chip



- ❑ <https://www.youtube.com/watch?v=OyEYA8kNFZM>
- ❑ <https://www.youtube.com/watch?v=Hi7rK0hZnfc>
- ❑ <https://www.youtube.com/watch?v=-aQH0ybMd3U>

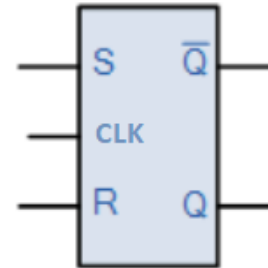
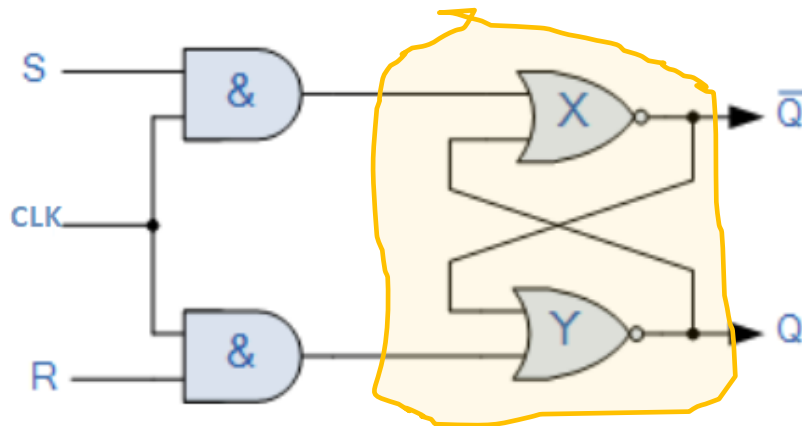
Gated/Clocked Flipflop

- It is sometimes desirable in sequential logic circuits to have SR flip-flop that only changes state when certain conditions are met regardless of the condition of either the Set or the Reset inputs.
- By connecting a 2-input AND gate in series with each input terminal of the SR Flip-flop a Gated SR Flip-flop can be created.
- The addition of this input means that the output at Q only changes state when it (third input) is HIGH.
- We can use Clock Pulse (CLK) as a gate input making it Clocked Flip flop as shown below.
 - ▣ Rising edge Triggered (Positive Edge)
 - ▣ Falling Edge Triggered (Negative Edge)



Clocked RS Flipflop

Gated/Clocked RS Flip flop



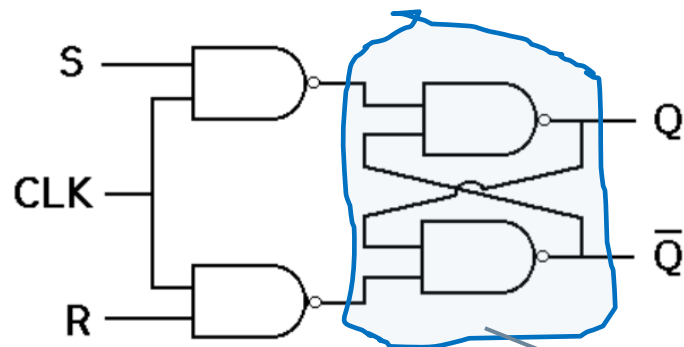
Characteristic Table

**Clock (CLK)
used as Gate**

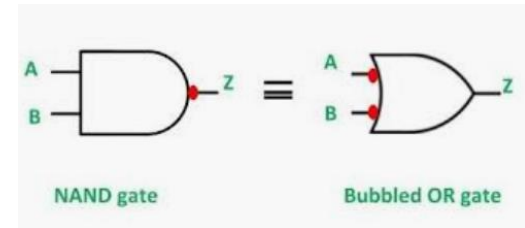
Active High RS Latch

Clk	S	R	Q(t+1)	
0	X	X	Q(t)	No change
1	0	0	Q(t)	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	?	Undefined

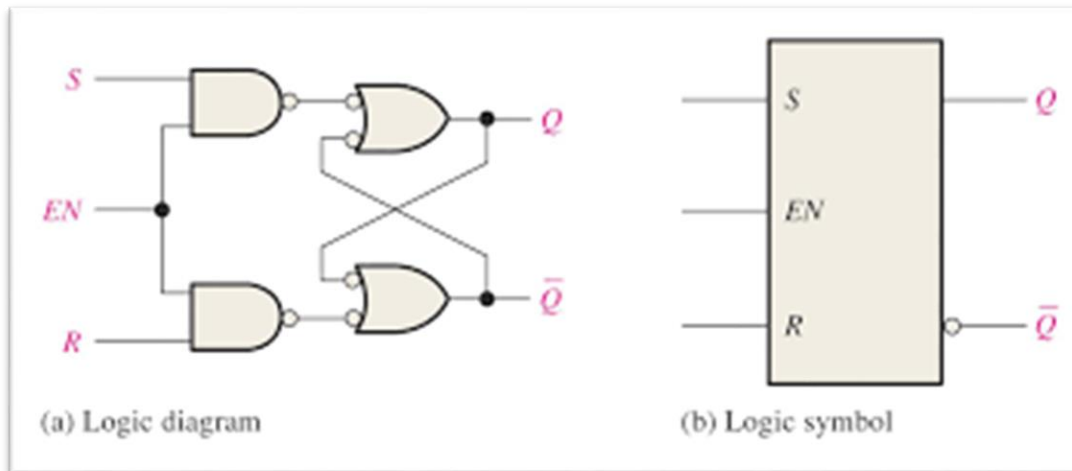
More on Clocked RS flip flop



Active Low RS Latch



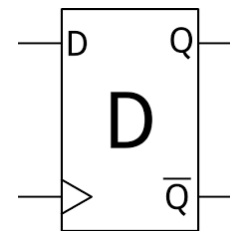
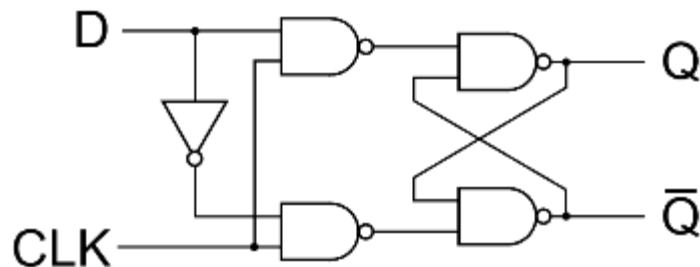
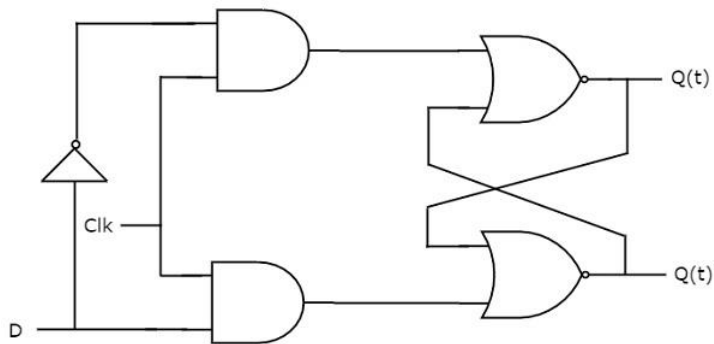
DeMorgan's Equivalent



From Digital Fundamentals by Floyd (Page No. 296)

Clocked D Flipflop

- The D Flop flop is modification of RS Flip flop. (D stands for Data)
- The problem of undefined output in SR Flip flop, when both R and S become 1 gets avoided in D Flip flop. The simple solution to avoid such condition is by providing just a single input. Thus, the non clocked input to AND gates are guaranteed to be opposite of each other by inserting an inverter between them.

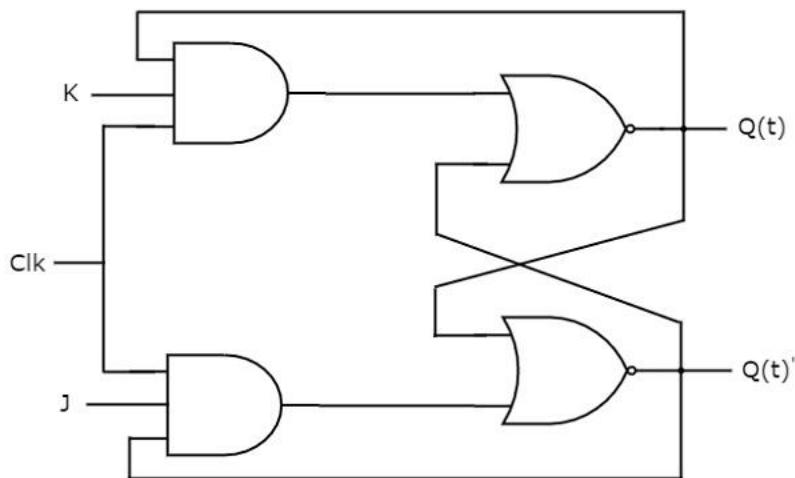


Characteristic Table

Clk	D	Q(t+1)	
0	X	Q(t)	No change
1	0	0	Clear
1	1	1	Set

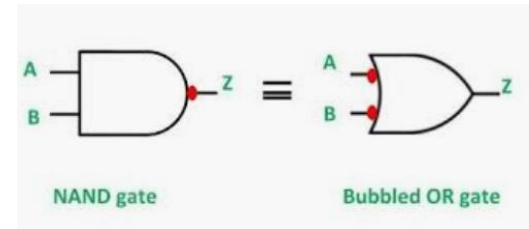
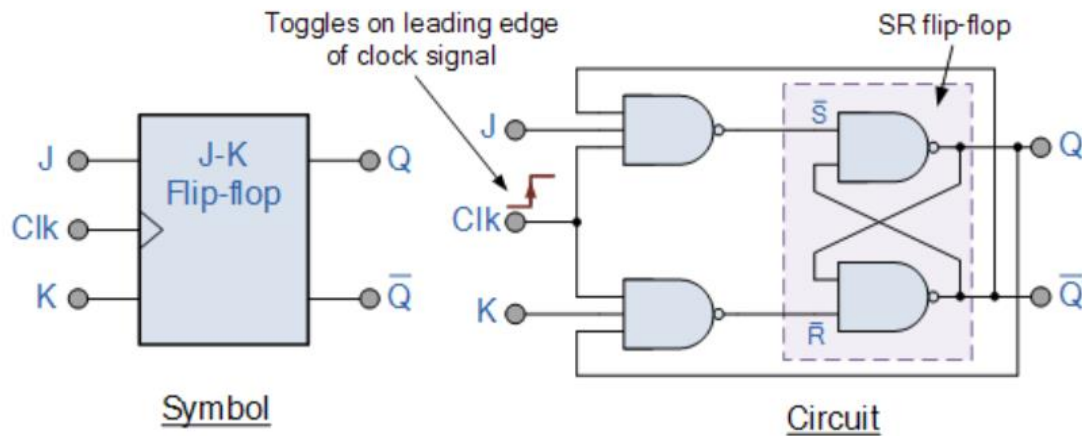
J K Flip flop

- Invented by Jack Kilby
- A JK is refinement of RS Flipflop in that the indeterminate state of the RS type is defined in the JK type.
- The inputs J and K behave exactly like inputs S and R to Set and reset Flip flop respectively. When J and K are 1, the Flip flop output is complemented with clock transaction.

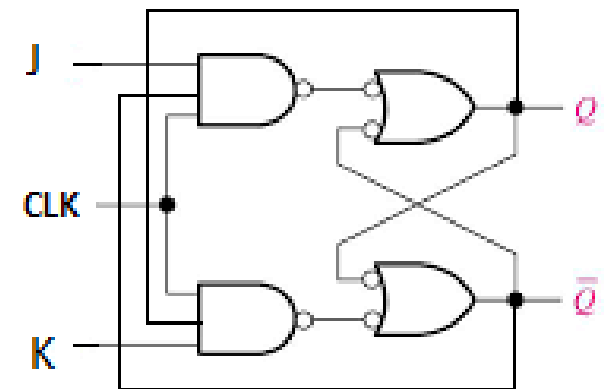


Clk	J	K	$Q(t+1)$	
0	X	X	$Q(t)$	No change
1	0	0	$Q(t)$	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$Q'(t)$	Compliment

More on JK flip flop



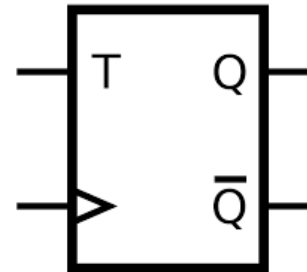
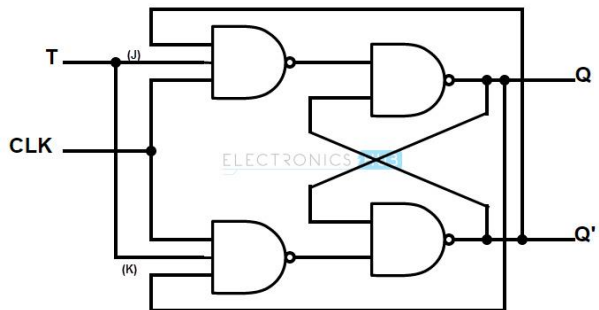
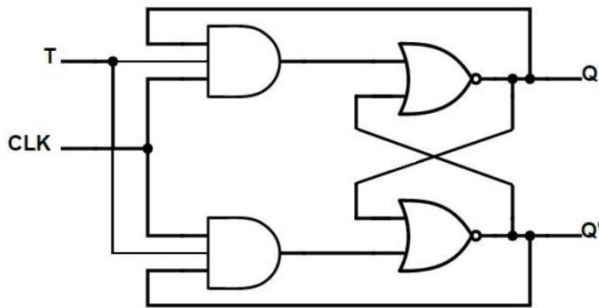
DeMorgan's Equivalent



Race-around Condition in JK FF ?

T Flip flop

- T(Toggle) Flipflop is obtained from JK Flip flop by joining inputs J and K together. The implementation of T Flipflop is shown in figure.
- When $T=0$, clock pulse transition does not change the state.
- When $T=1$, the clock pulse transition complement the state of the flip flop.



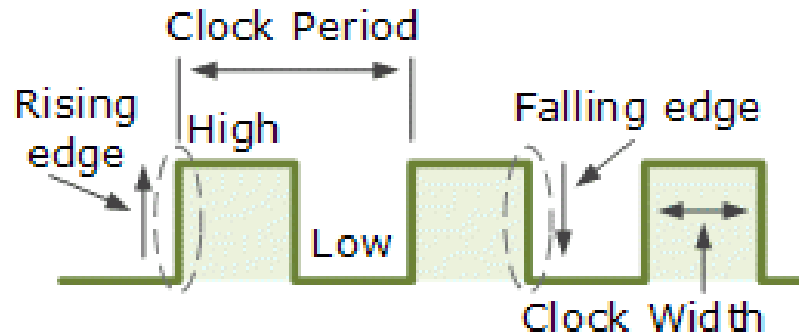
Clk	T	$Q(t+1)$	
0	X	$Q(t)$	No change
1	0	$Q(t)$	No change
1	1	$Q'(t)$	Complement

Race Condition



Triggering of Flipflops

- The clocked Flip flops are triggered during the positive edge of pulse, and the state transition starts as soon as the pulse reaches the logic **1** level
- The new state of the Flip flop may appear at the output terminals while the input pulse is still **1**.
- If the other inputs of the Flip flop change while the clock is still **1**, the Flip flop will start responding to these new values and new output state may occur. → This poses a problem
- If we can make a Flip flop which responds to the +ve (or -ve) **edge transition** only, instead of entire pulse duration, then the multiple transition problem can be eliminated.



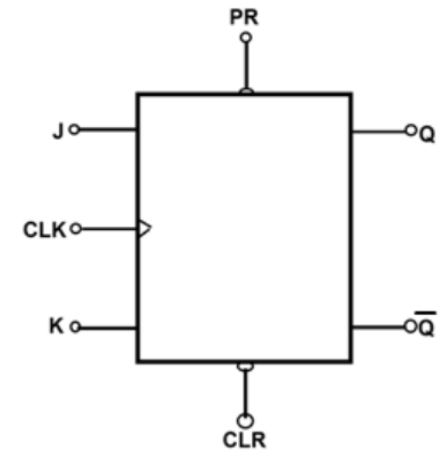
Edge Triggered Flip flops

□ Positive Edge Triggered FF

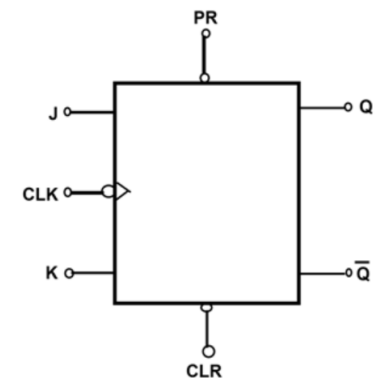
In positive edge triggered Flip Flops clock samples the input line at the positive edge (rising edge or leading edge) of the clock pulse. The state of output of the FF is set or Reset depending upon the state of the input at positive edge of the clock. The state of the output remains for one clock cycle and clock again samples the input line on the next positive edge of the clock.

□ Negative Edge Triggered FF

In Negative edge triggered Flip Flops clock samples the input line at the negative edge (falling edge or trailing edge) of the clock pulse. The state of output of the FF is set or Reset depending upon the state of the input at negative edge of the clock. The state of the output remains for one clock cycle and clock again samples the input line on the next negative edge of the clock.



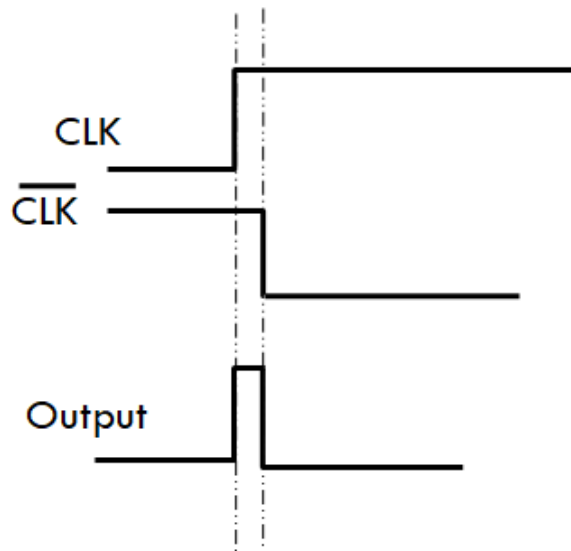
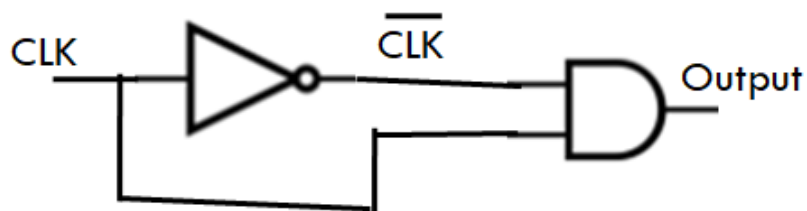
Positive Edge Triggered JK Flip Flop



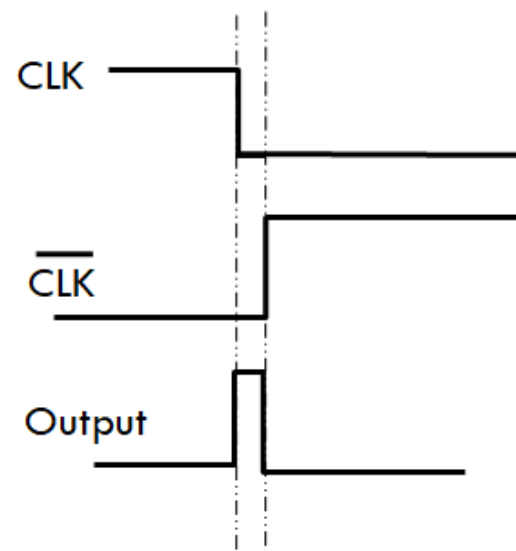
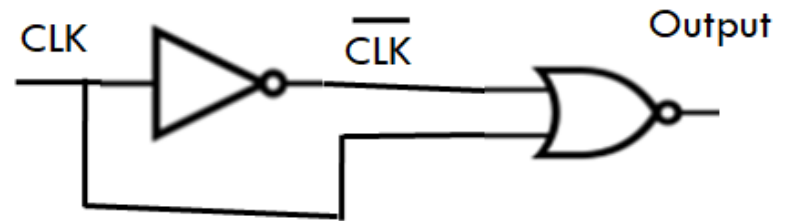
Negative Edge Triggered Flip Flop

Edge Detector Circuit

Rising Edge Detector



Falling Edge Detector



Excitation Table

- Operational Characteristics of FF is given by Characteristic table. The characteristic table specifies the next state of flip flop when the inputs and present state are known.
inputs + Present state \rightarrow next state
- Excitation Table shows “For a particular transition to take place what should be the inputs” e.g., if present state is 0 and to get next state as 1 what should be the inputs
- Excitation Table for RS Flipflop

Present State	Next State	SR flip-flop inputs	
Q(t)	Q(t+1)	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Excitation Table

Present State	Next State	JK flip-flop inputs	
Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Present State	Next State	D flip-flop input
Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State	Next State	T flip-flop input
Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

Conversion of Flipflops

- Steps for the conversions
 - Step 1: Write the Truth Table of the Desired Flip-Flop
 - Step 2: Obtain the Excitation Table for the given Flip-Flop from its Truth Table
 - Step 3: Append the Excitation Table of the given Flip-Flop to the Truth Table of the Desired Flip-Flop Appropriately to obtain Conversion Table
 - Step 4: Simplify the Expressions for the Inputs of the given Flip-Flop
 - Step 5: Design the Necessary Circuit and make the Connections accordingly

Convert D FlipFlop to T Flipflop

1. Truth Table for T Flip Flop

Input	Outputs	
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

2. Excitation Table for D Flip Flop

Outputs		Input
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

3. Conversion Table

T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

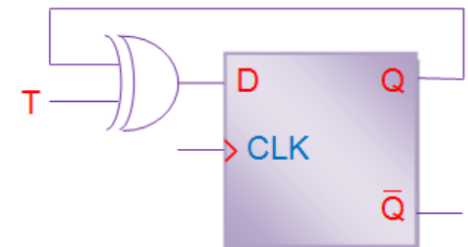
4. K-map Simplification

	Q_n	0	1
T	0	0 ⁰	1 ¹
	1	1 ²	0 ³

$$D = T\bar{Q}_n + \bar{T}Q_n$$

$$= T \oplus Q_n$$

5. Circuit Design



Convert T Flipflop to D Flipflop

1. Truth Table for D Flip Flop

Input	Outputs	
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

2. Excitation Table for T Flip Flop

Outputs		Input
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

3. Conversion Table

D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

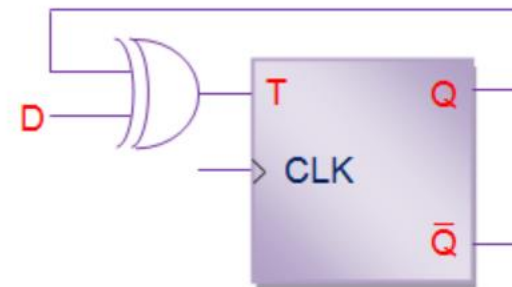
4. K-map Simplification

	Q_n	0	1
D	0	0 ⁰	1 ¹
	1	1 ²	0 ³

$$D = D\bar{Q}_n + \bar{D}Q_n$$

$$= D \oplus Q_n$$

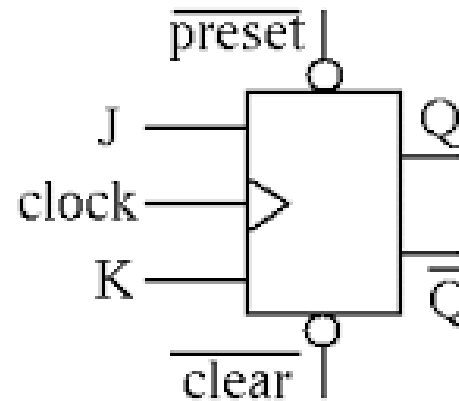
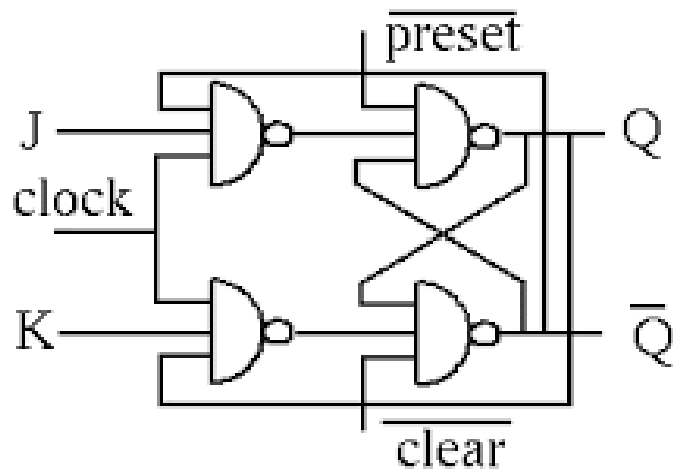
5. Circuit Design



Exercise

- Show the conversion of SR Flipflop to T Flipflop
- Show the conversion of D flipflop to JK flipflop

JK Flip Flop with Asynchronous Inputs



J	K	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	\overline{Q}_t

- The Pre and Clr inputs must both be kept High(1) for normal operation of JK flipflop
- If Pre =0 and Clr=1 $\rightarrow Q=1, Q'=0 \rightarrow$ Set
- If Pre=1 and Clr =0 $\rightarrow Q=0, Q'=1 \rightarrow$ Reset

SR Flip Flop with Asynchronous Inputs

